

Figure 1A

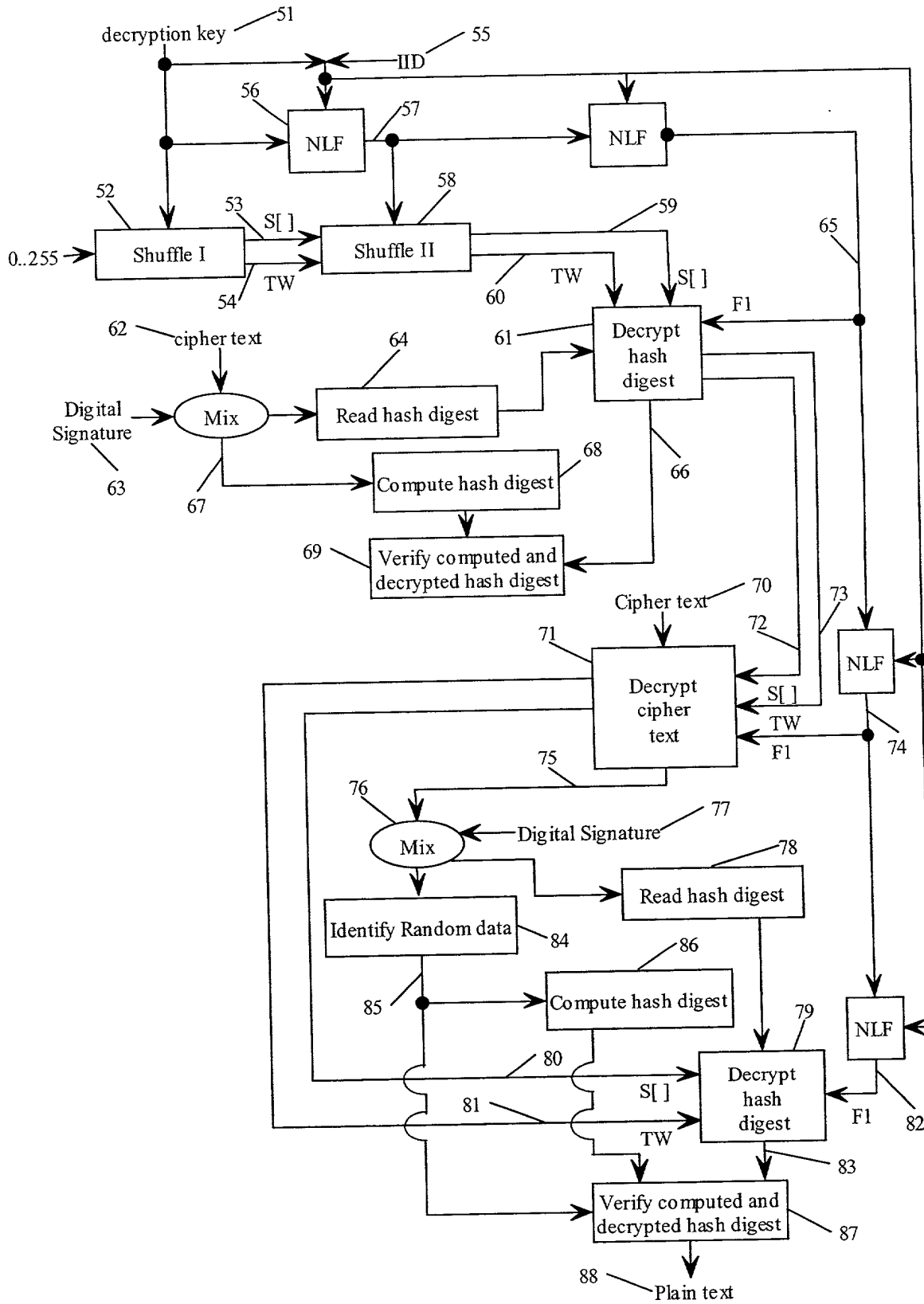


Figure 1B

Figure 2A

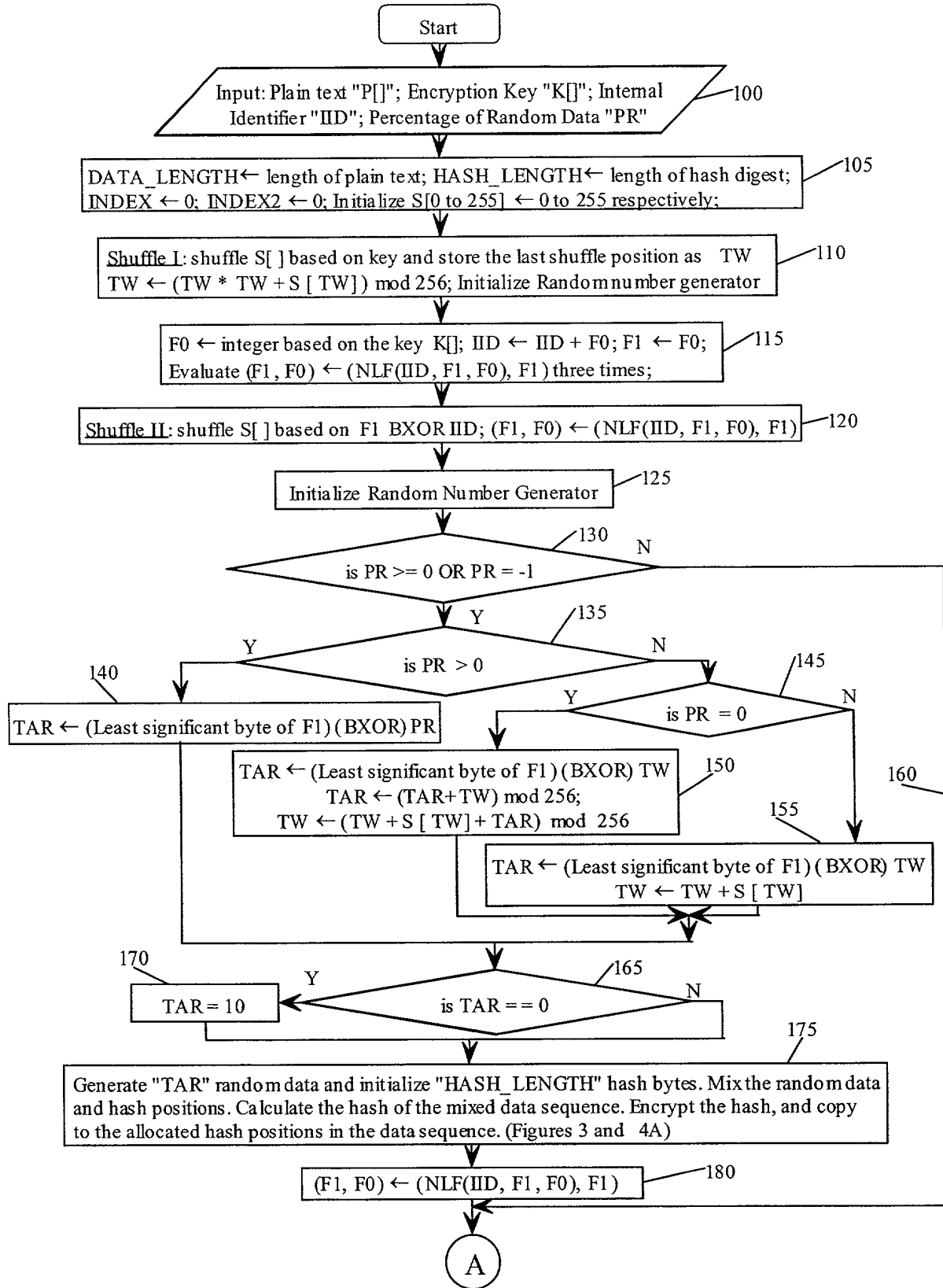
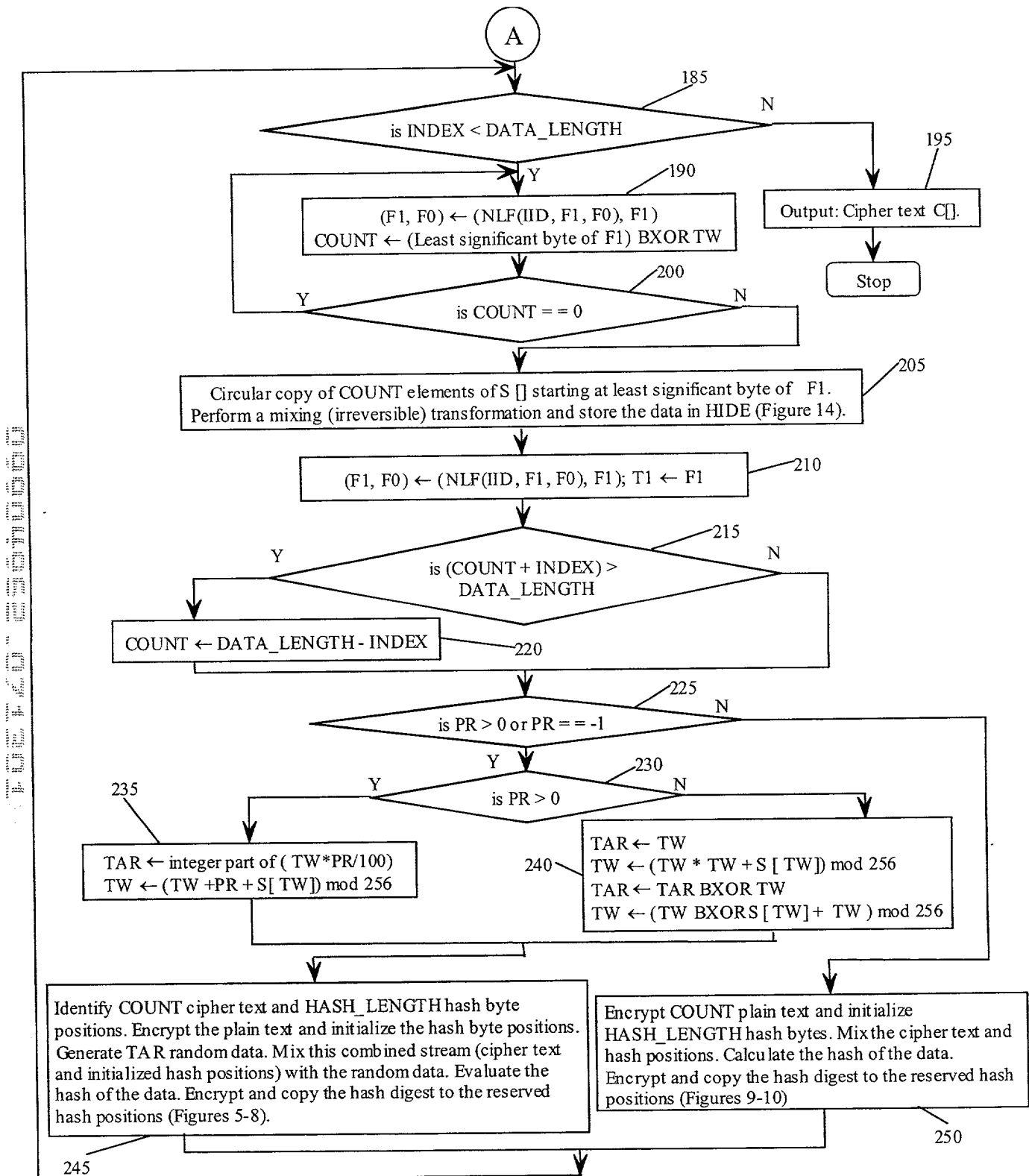


Figure 2B



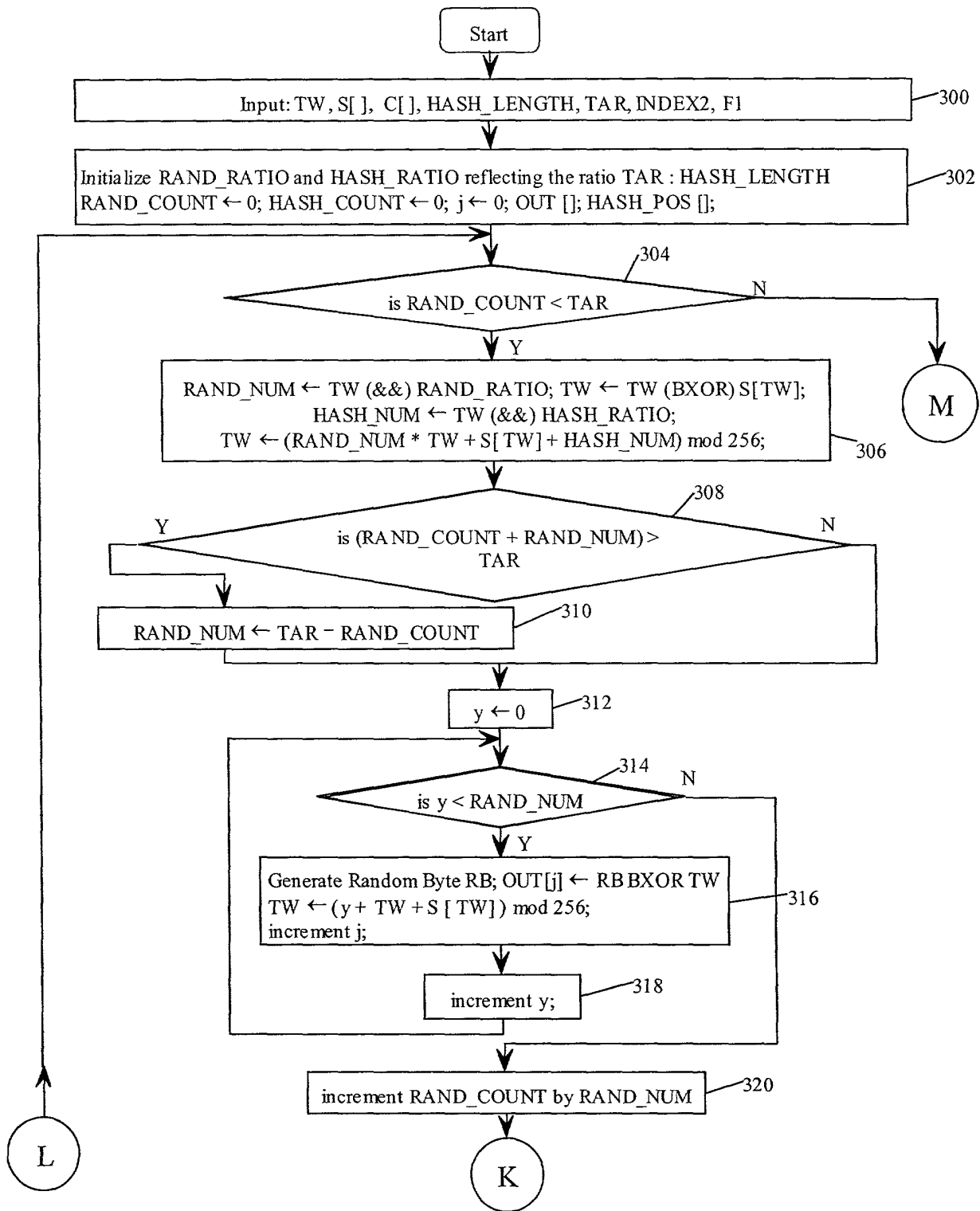


Figure 3

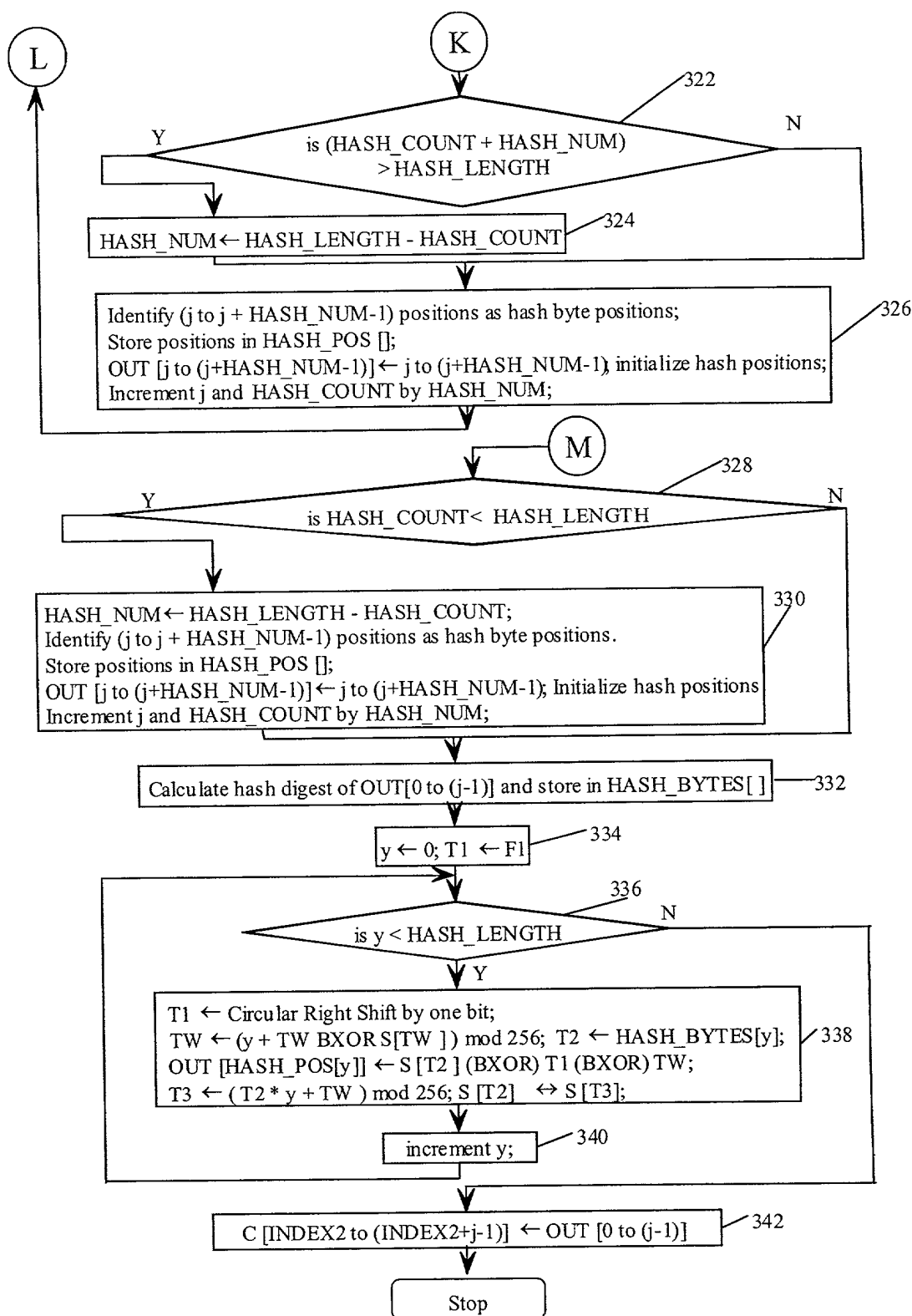


Figure 4A

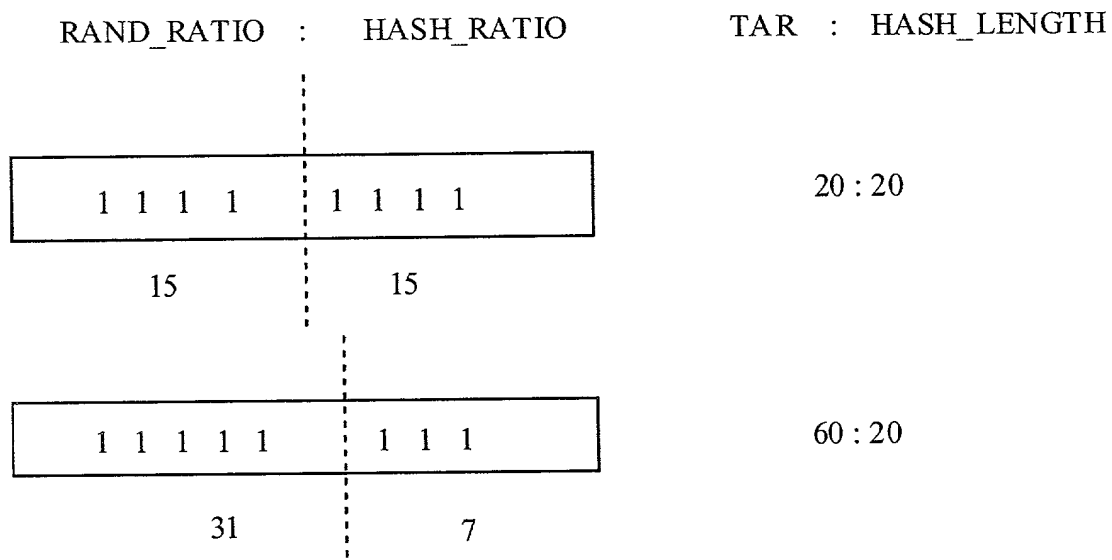


Figure 4B

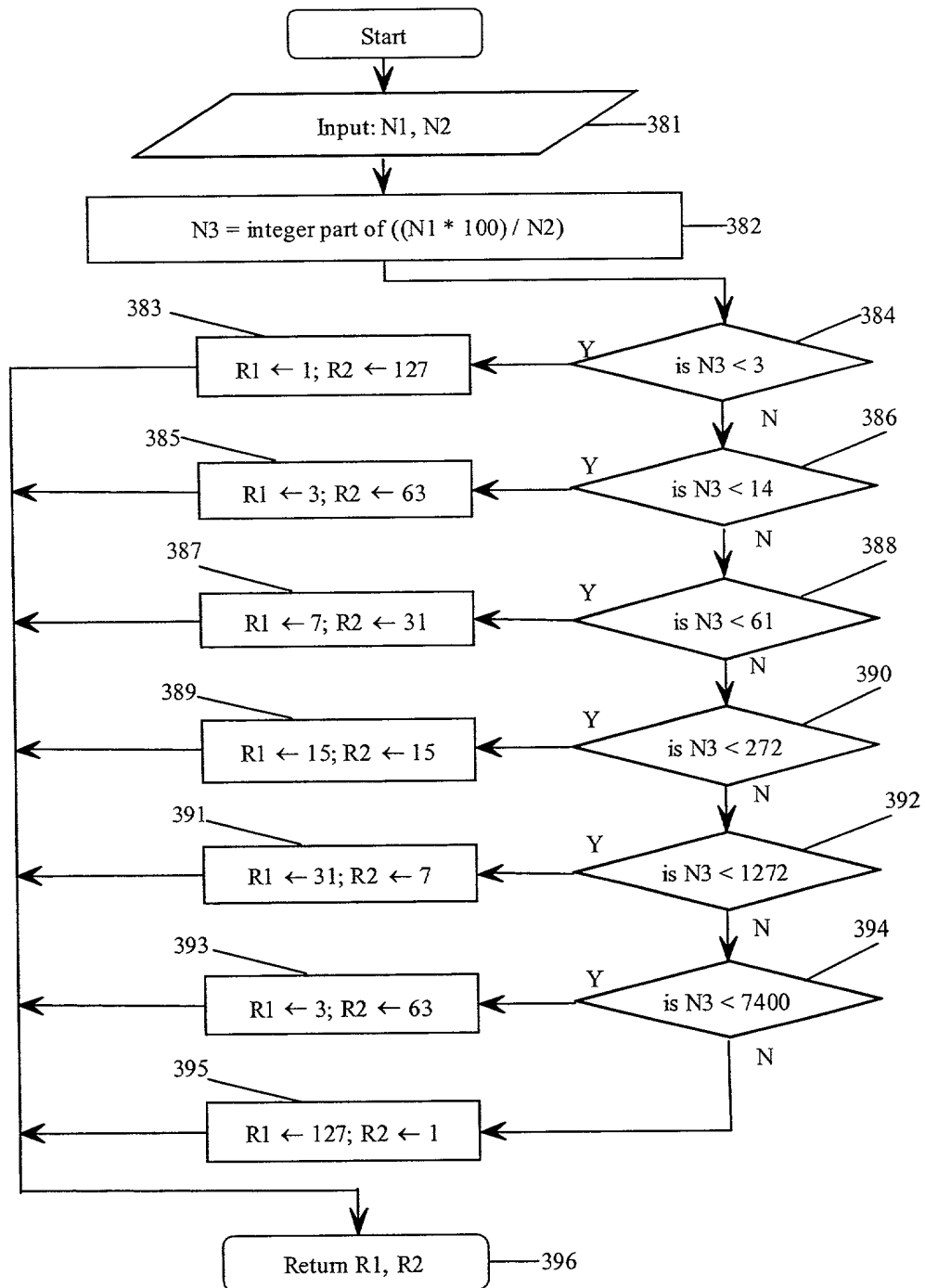


Figure 4C



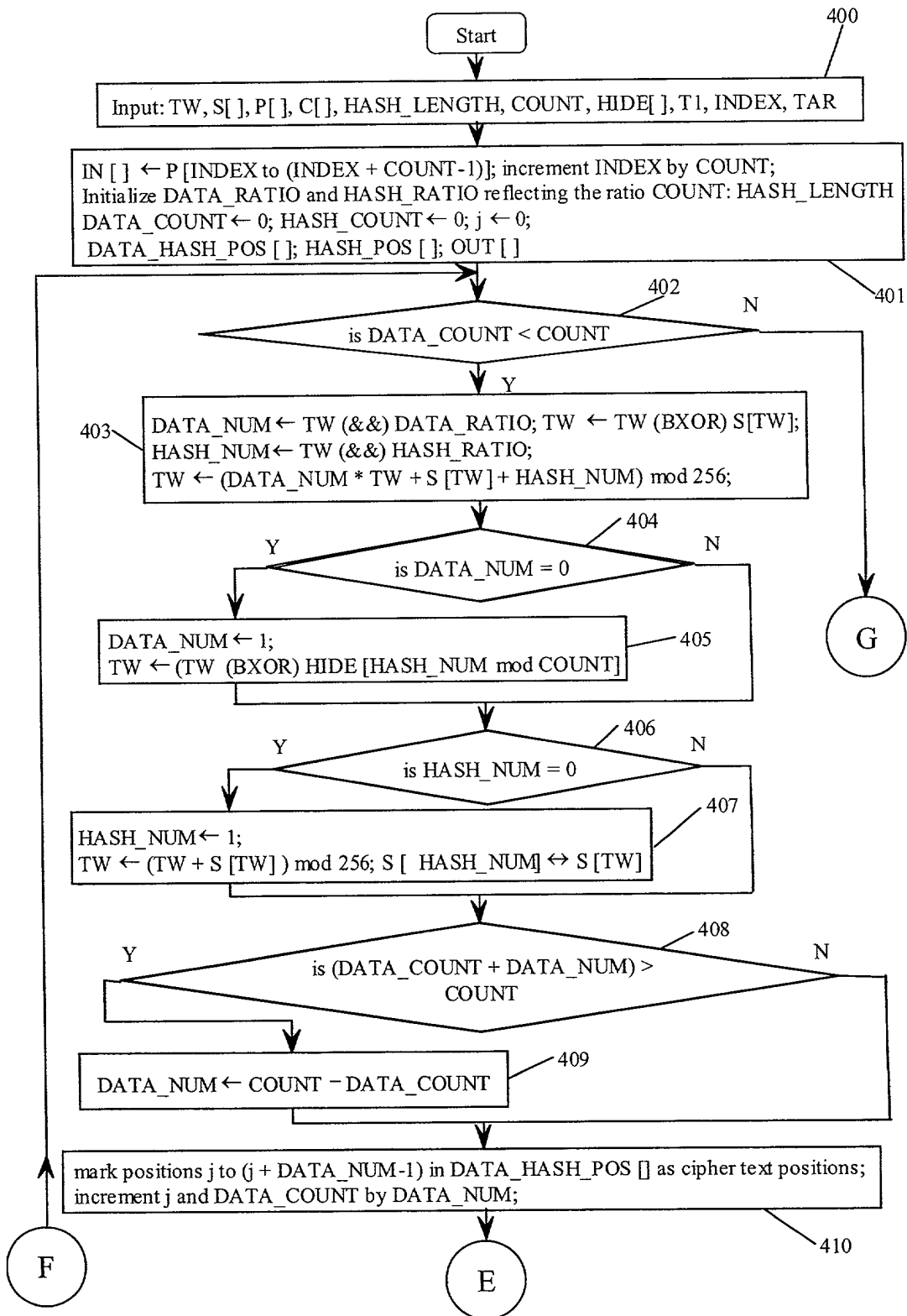


Figure 5

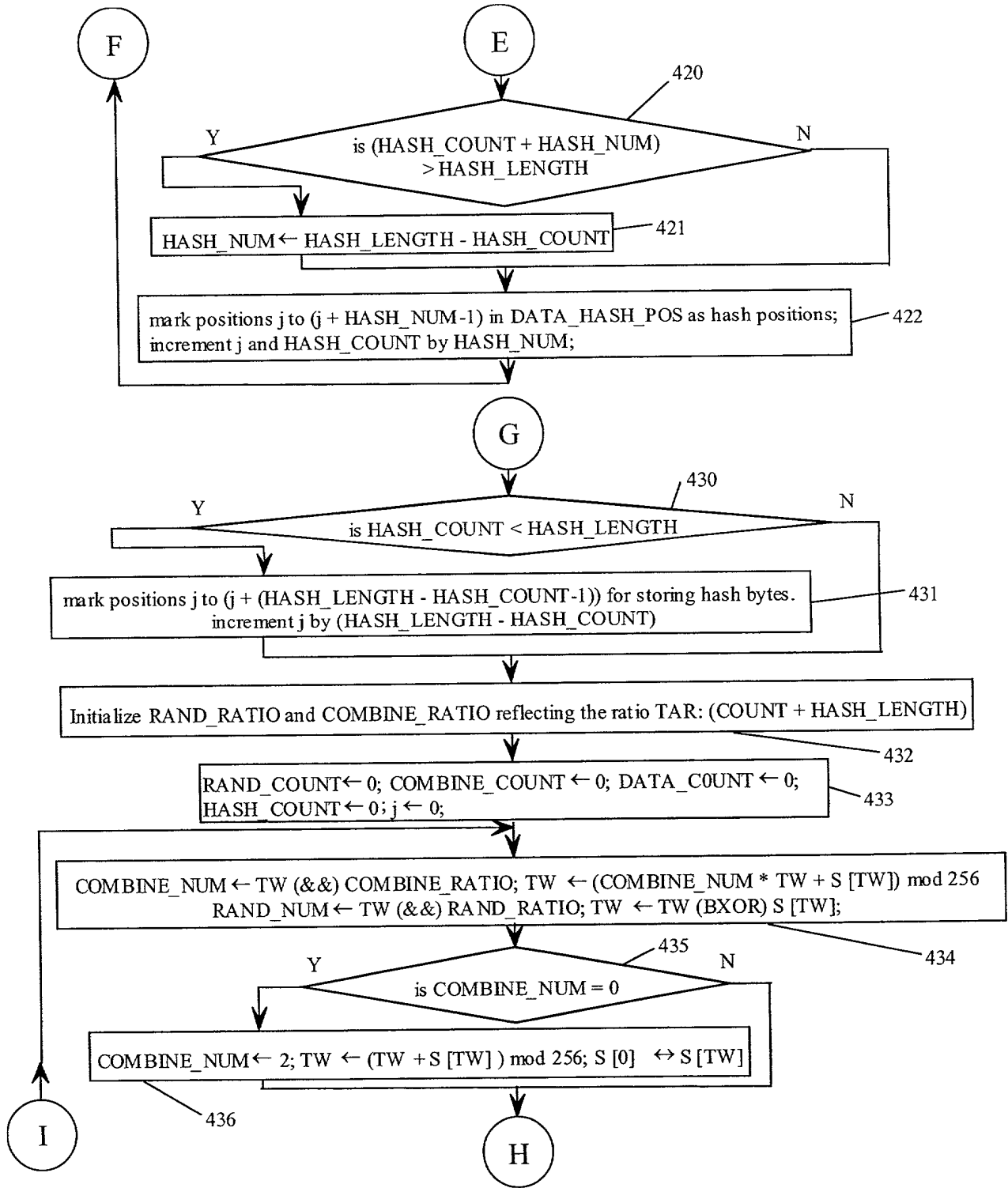


Figure 6

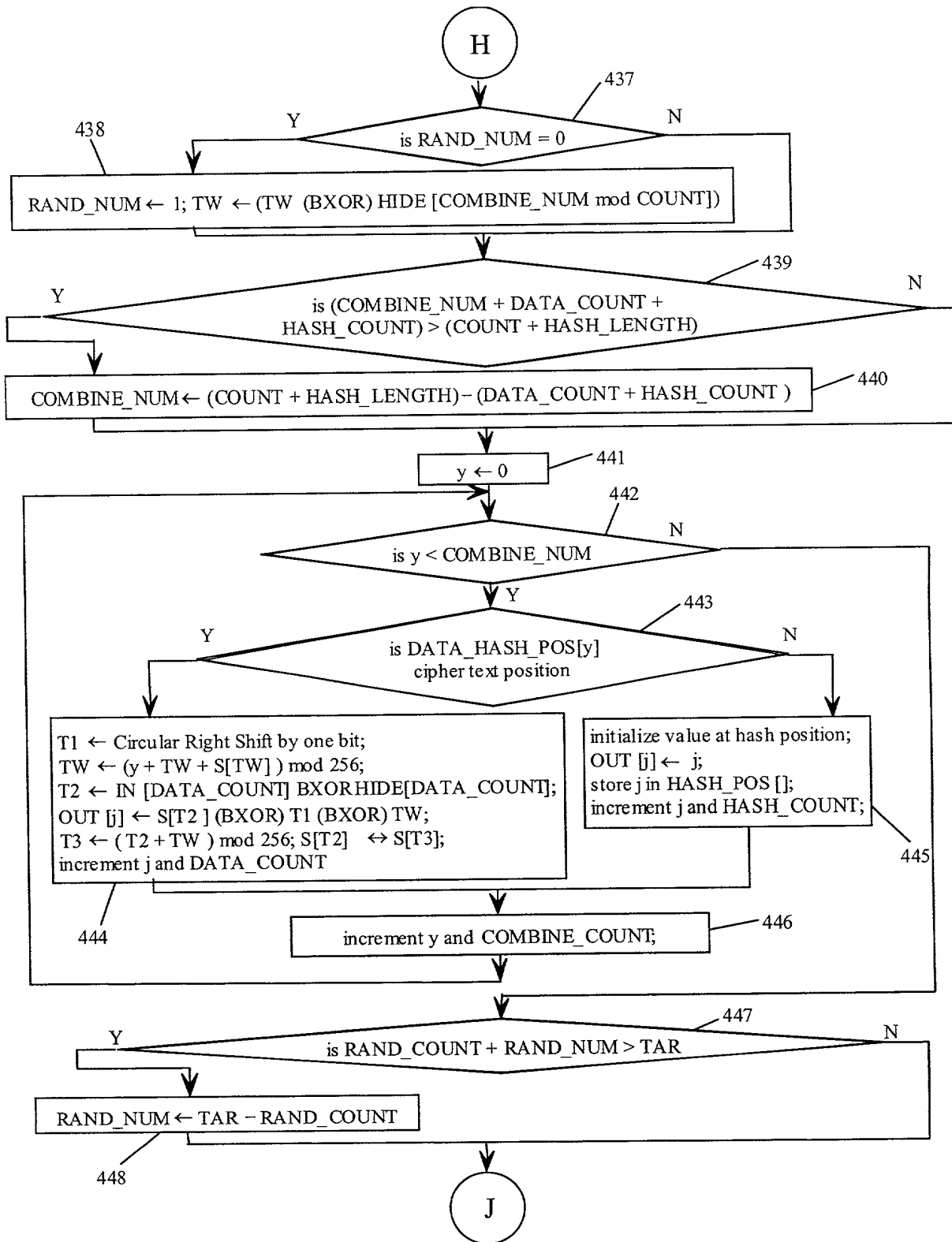


Figure 7

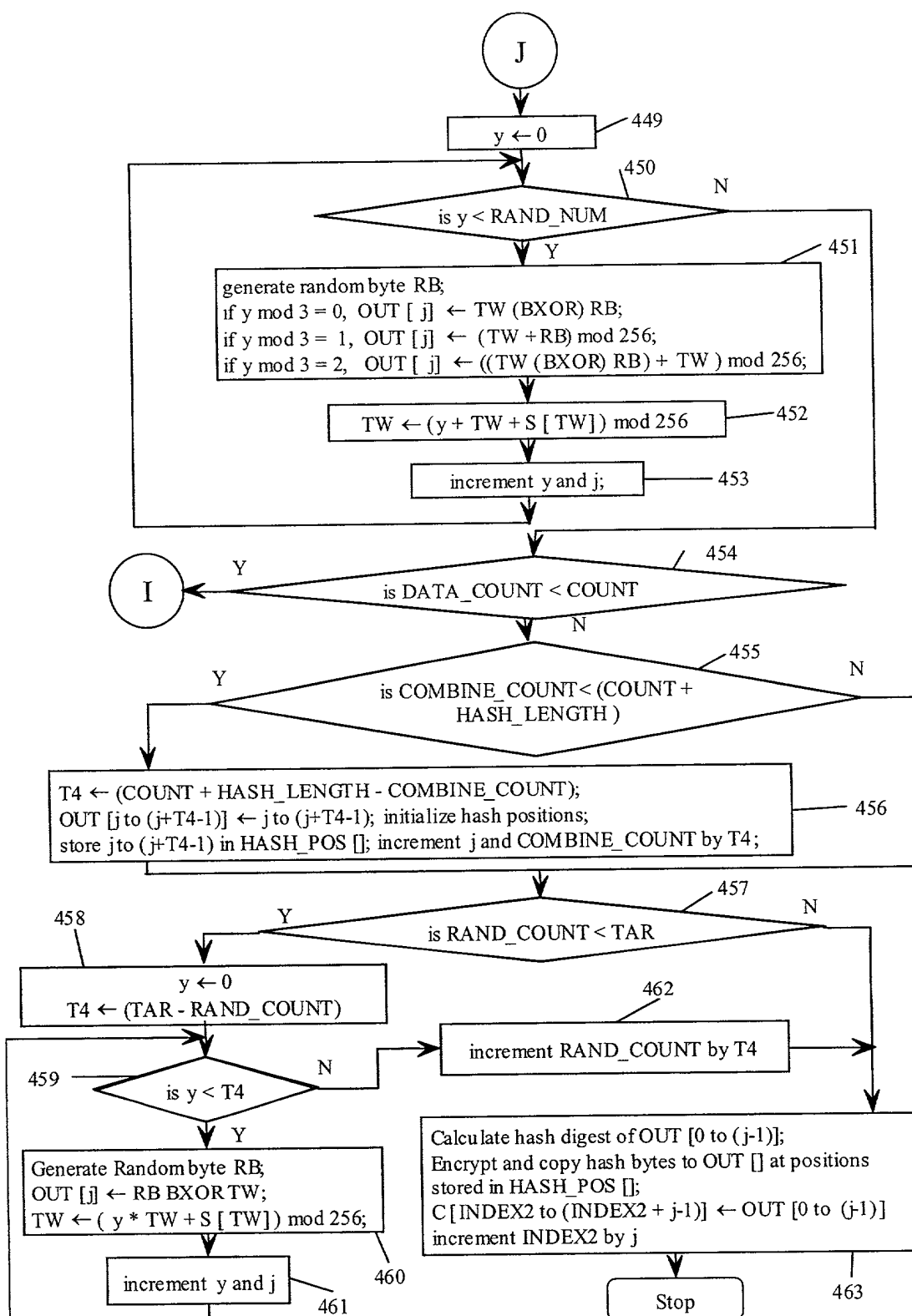


Figure 8

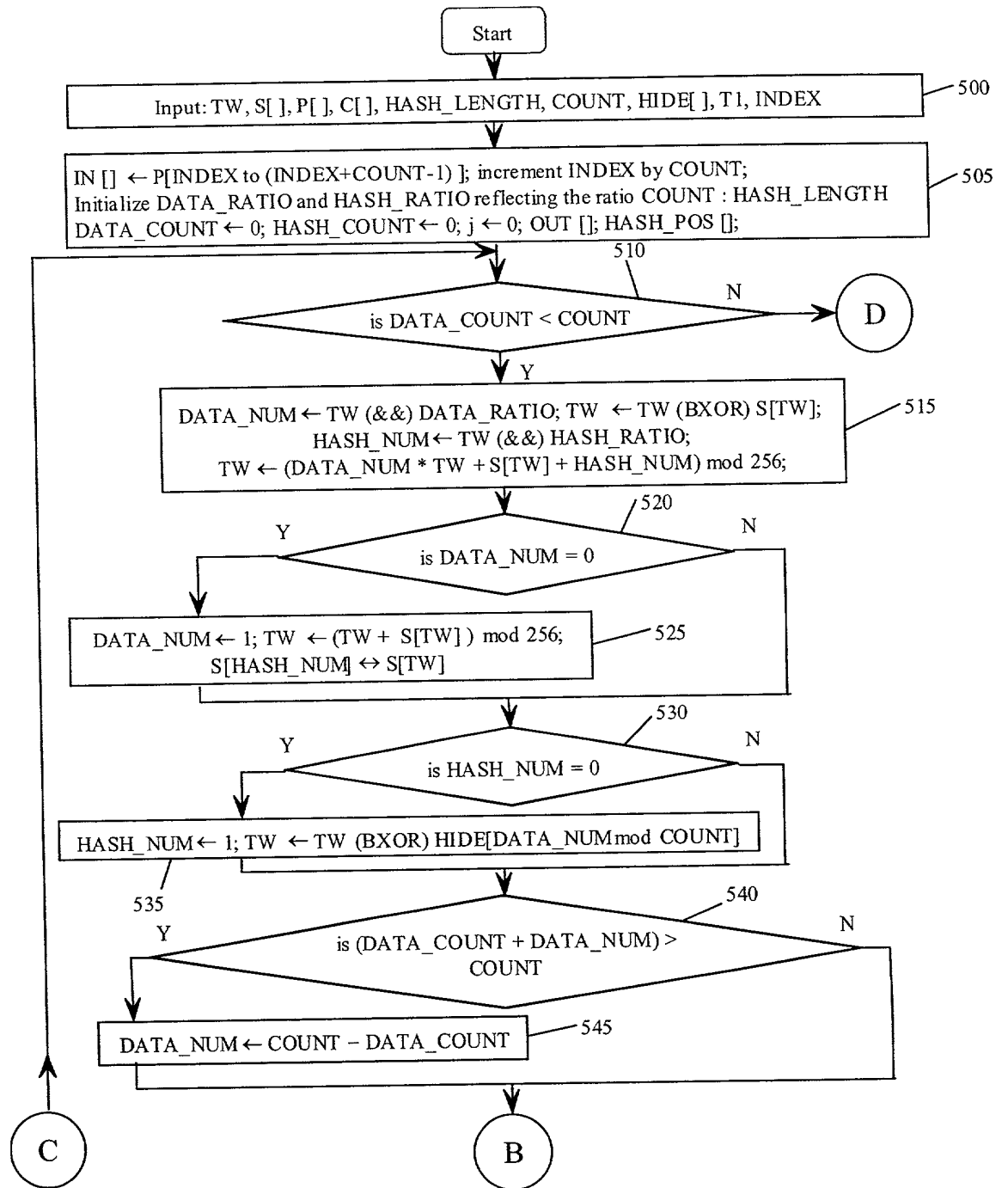
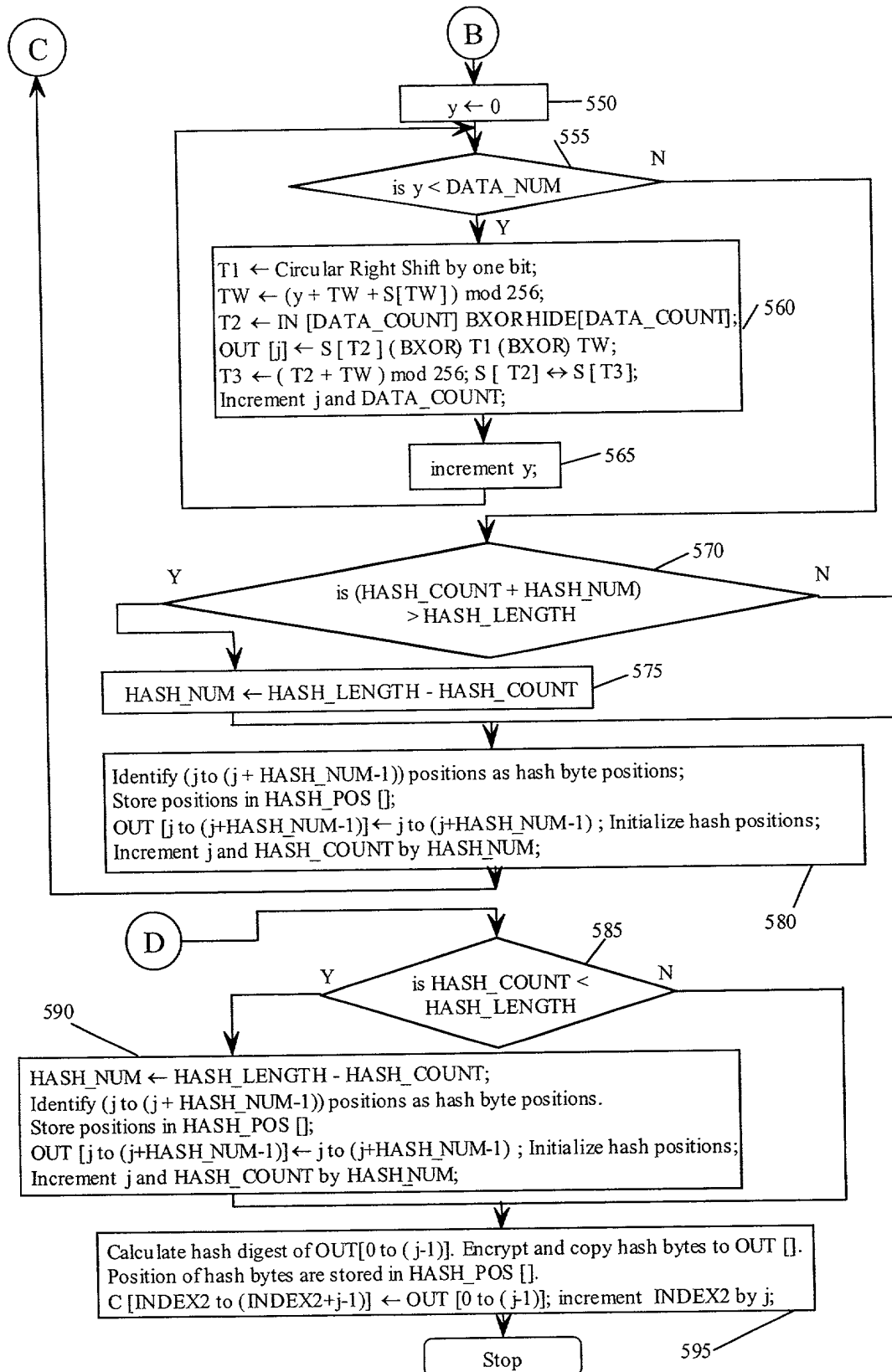
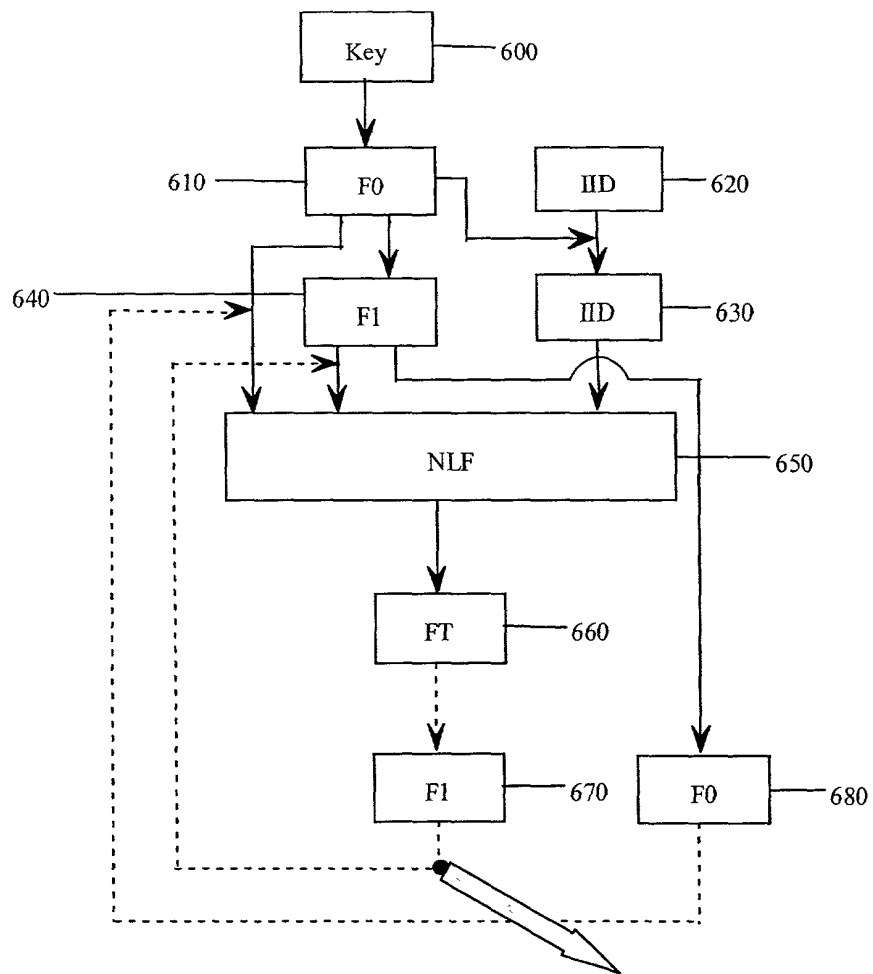


Figure 9



**Figure 10**



**Figure 11A**

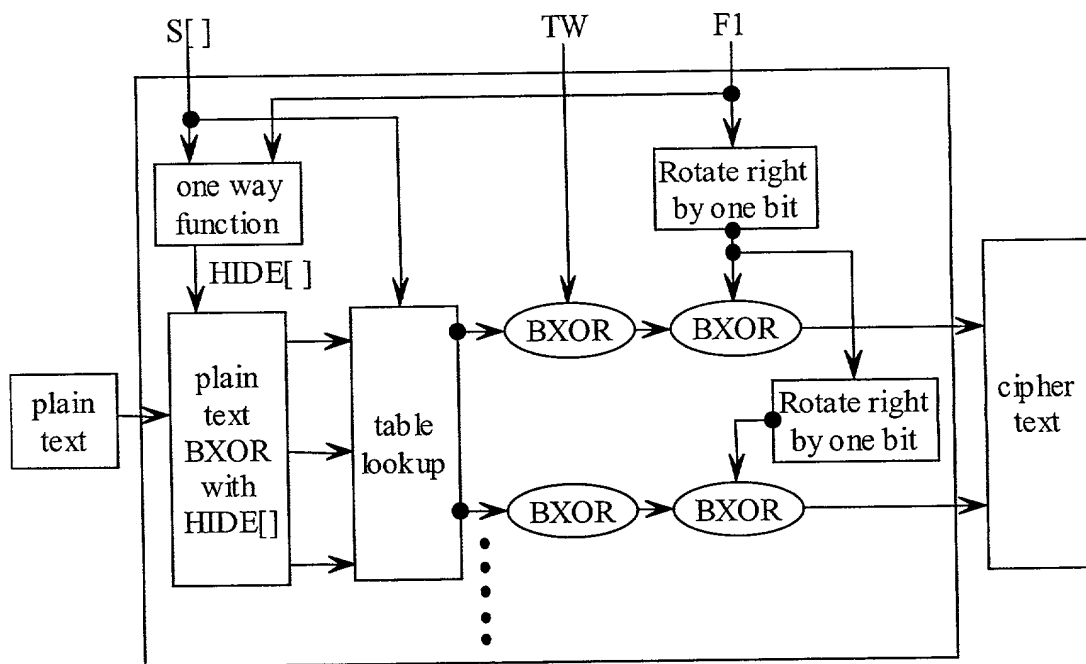
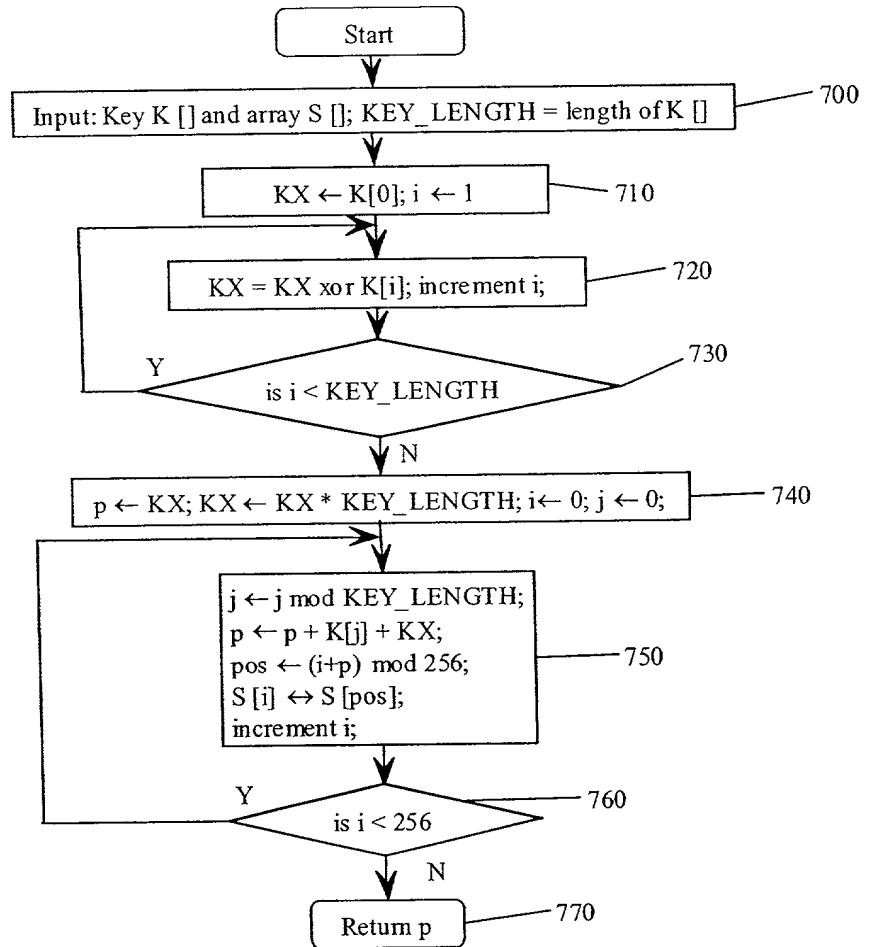
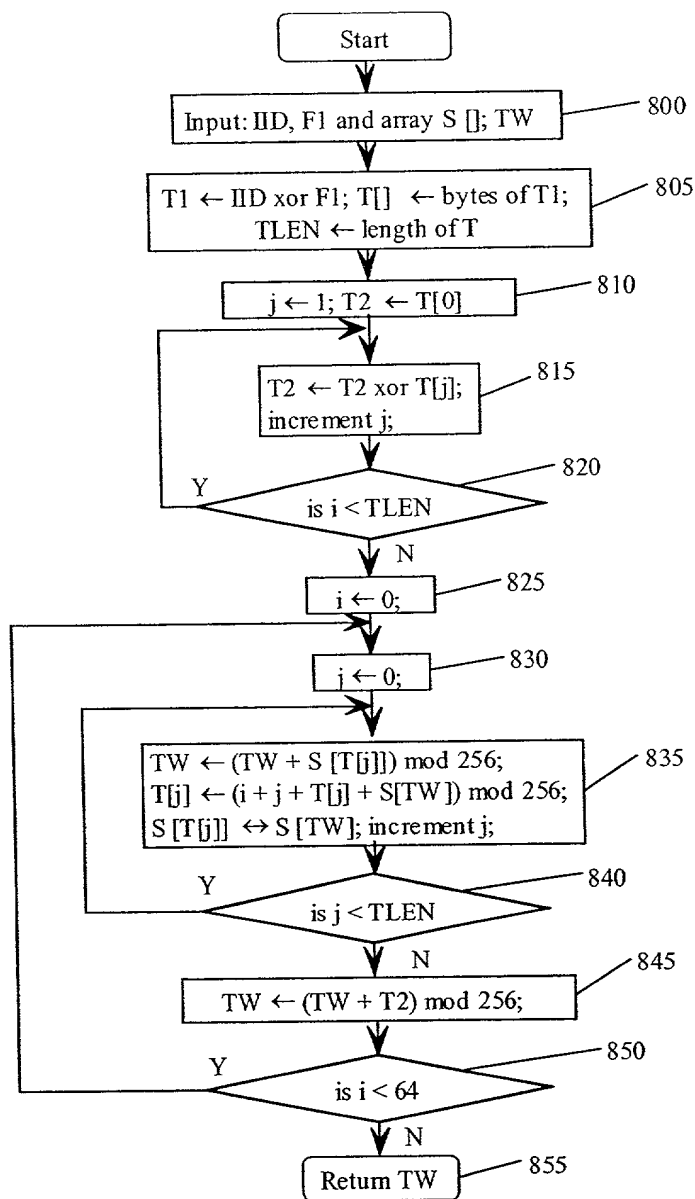


Figure 11B





**Figure 12**



**Figure 13**

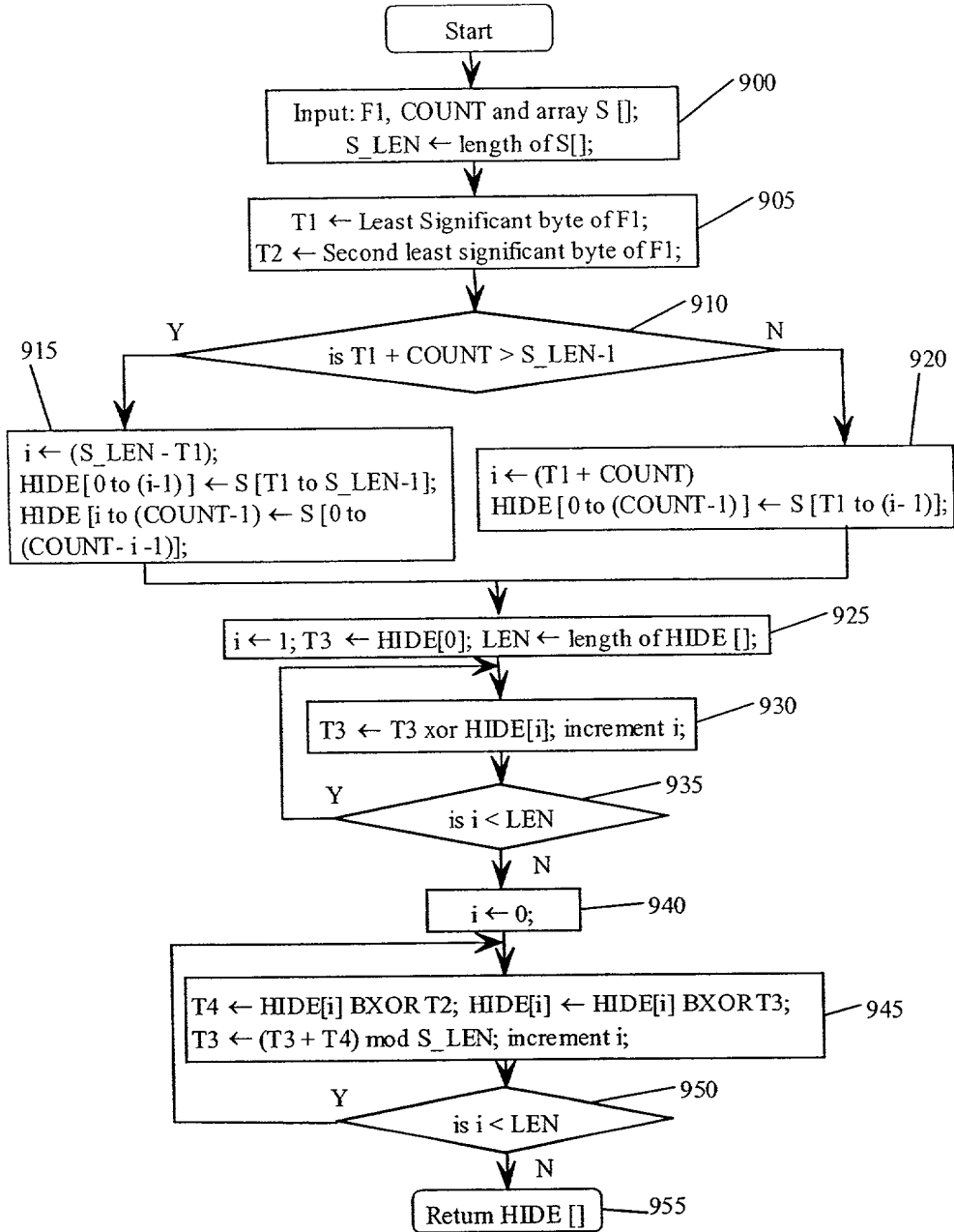


Figure 14

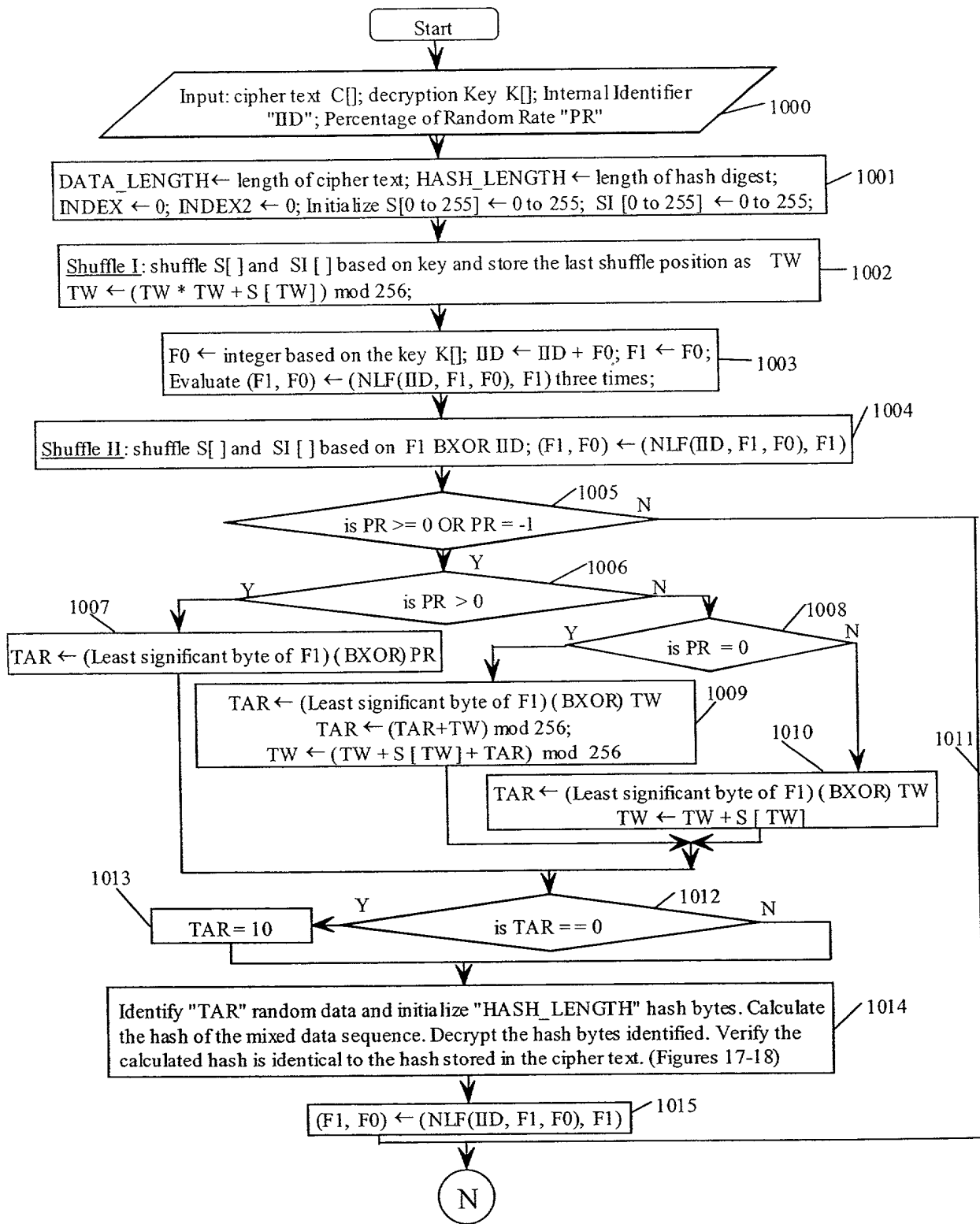


Figure 15

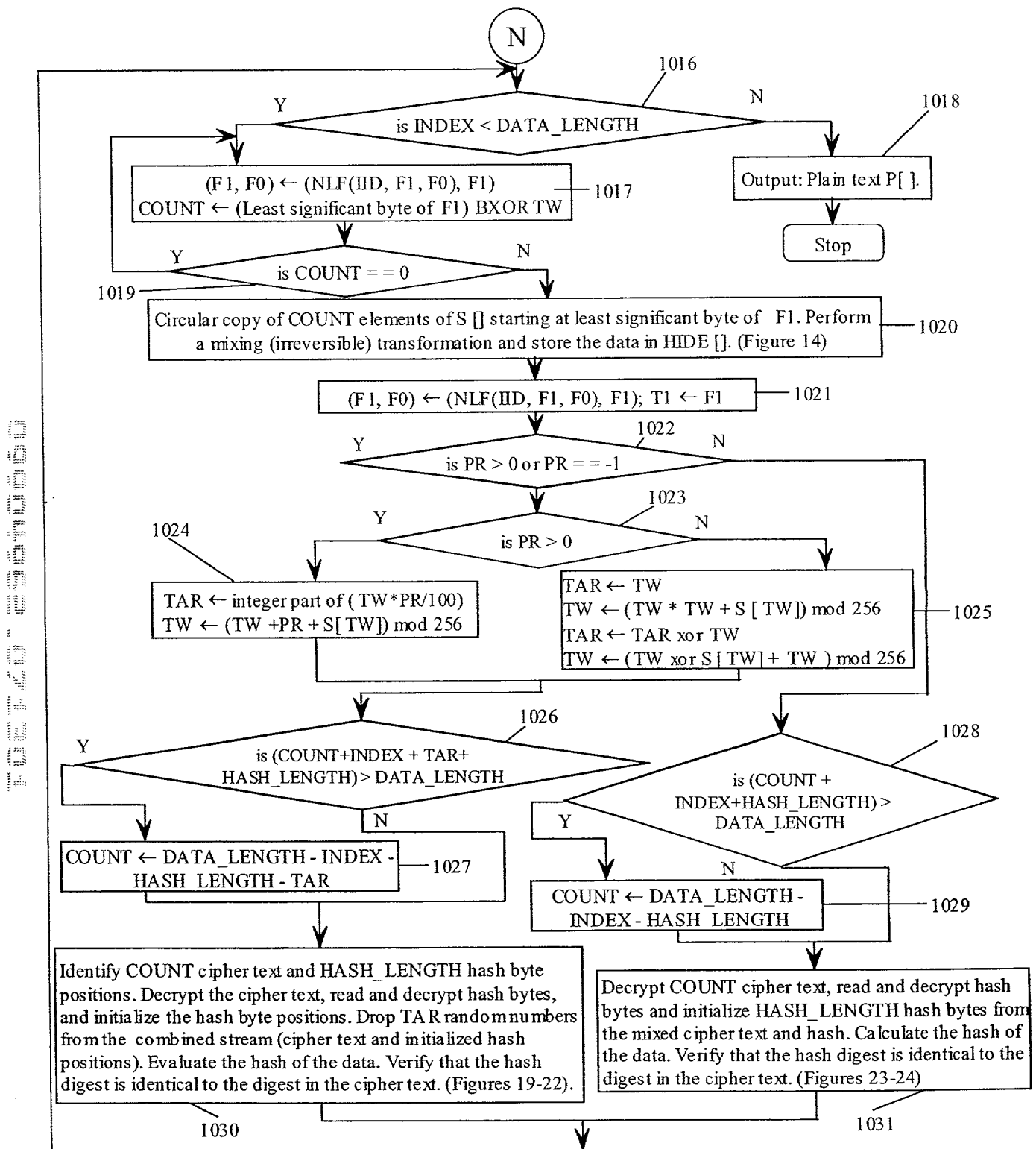


Figure 16

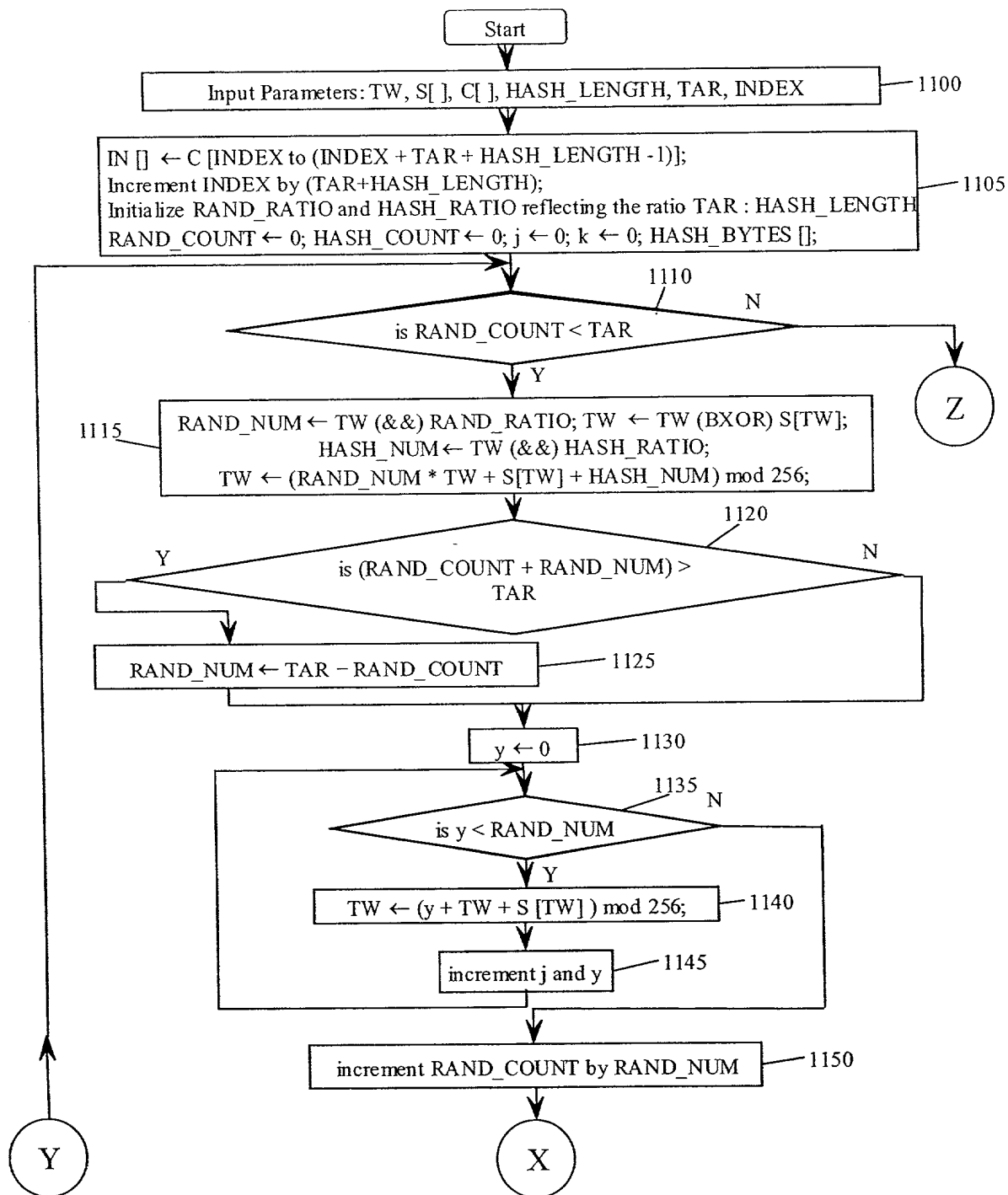


Figure 17

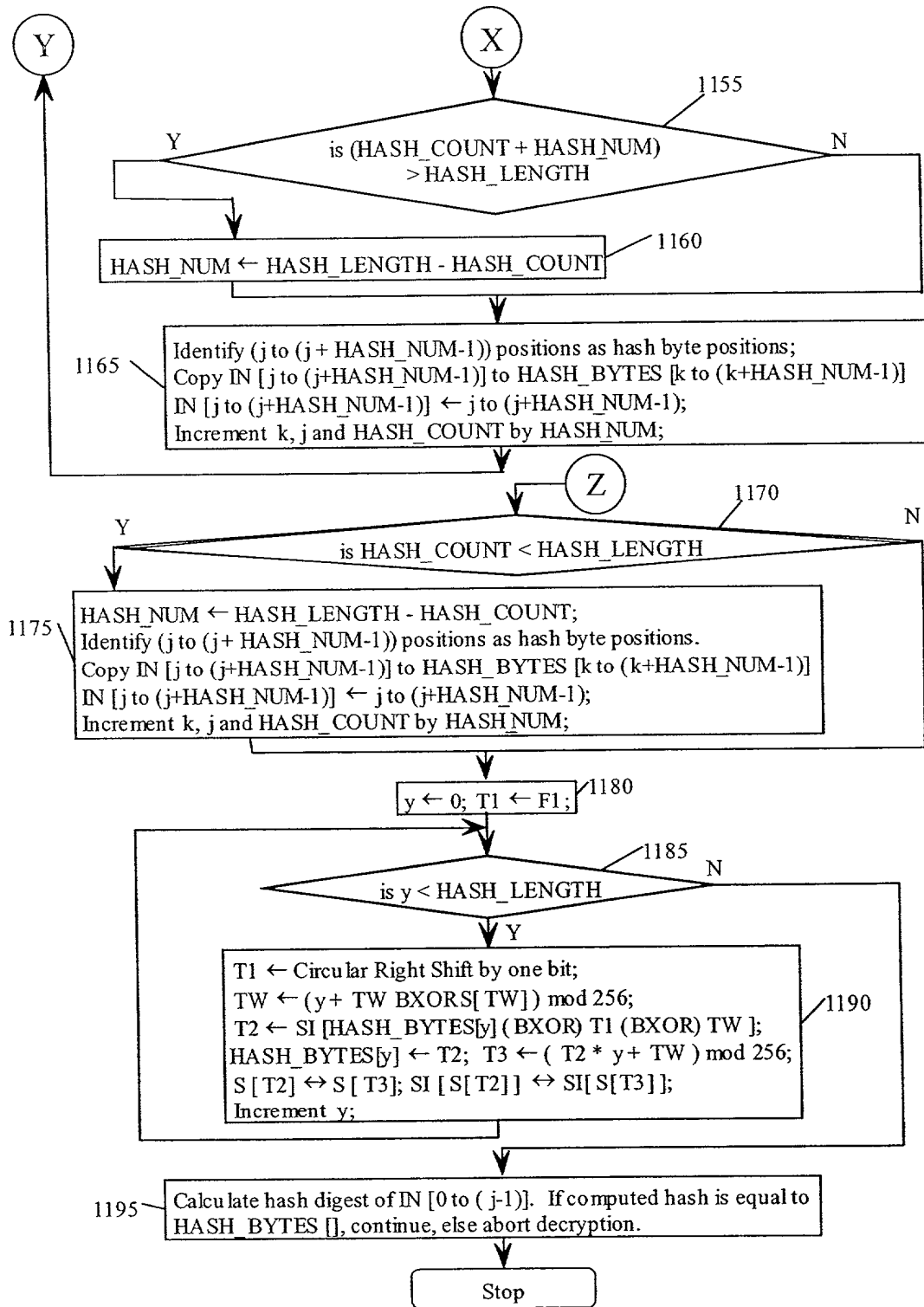


Figure 18

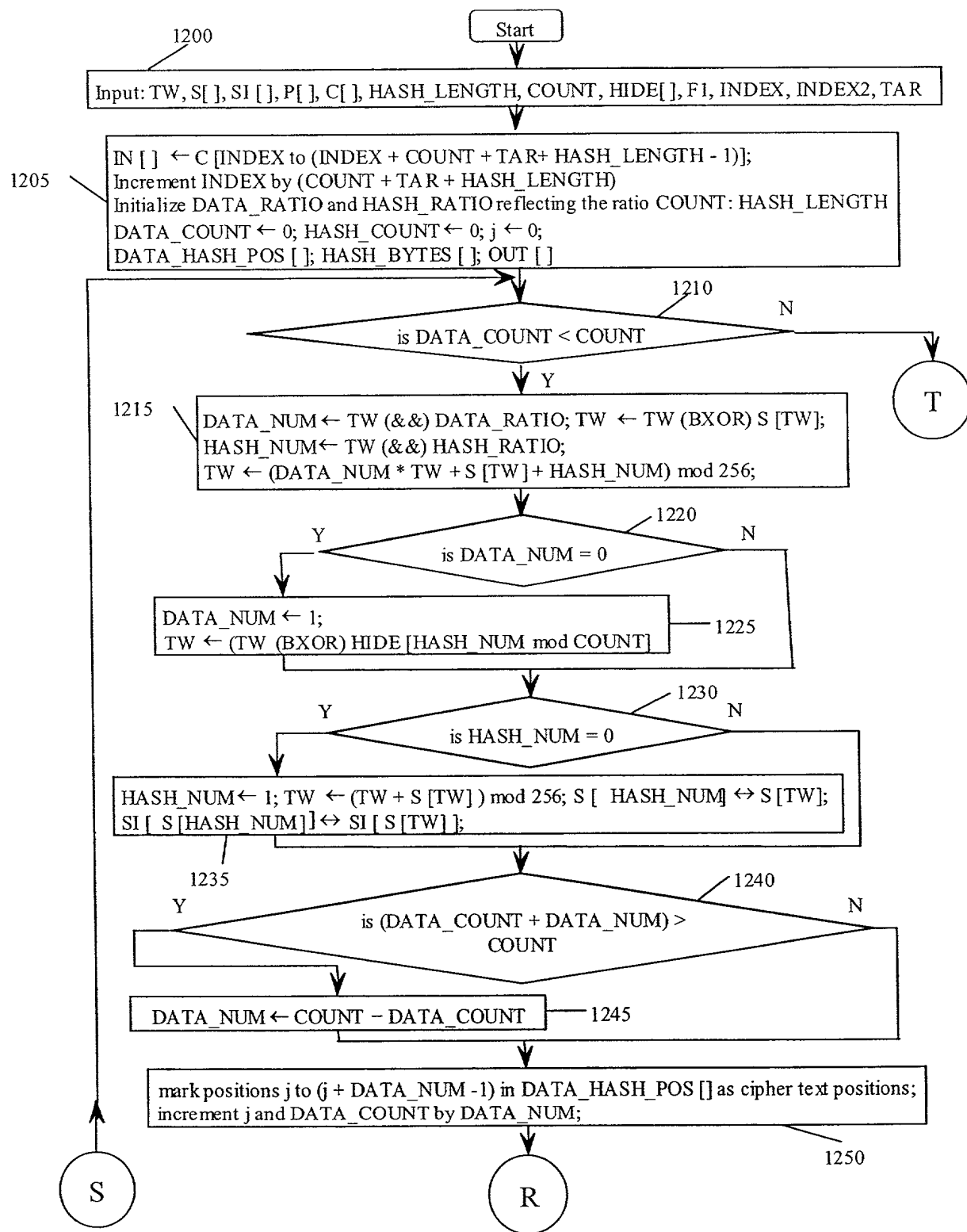


Figure 19



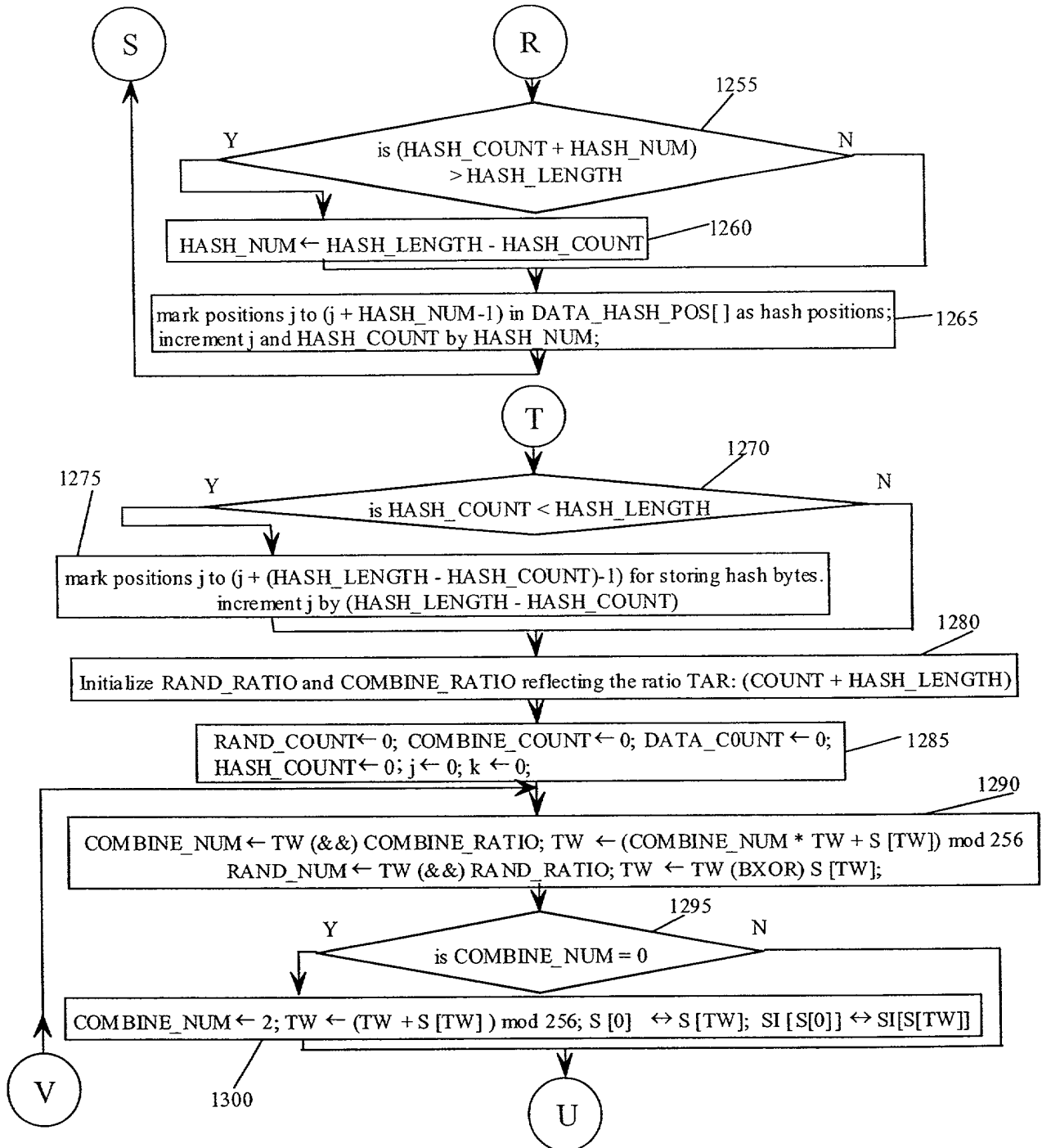


Figure 20

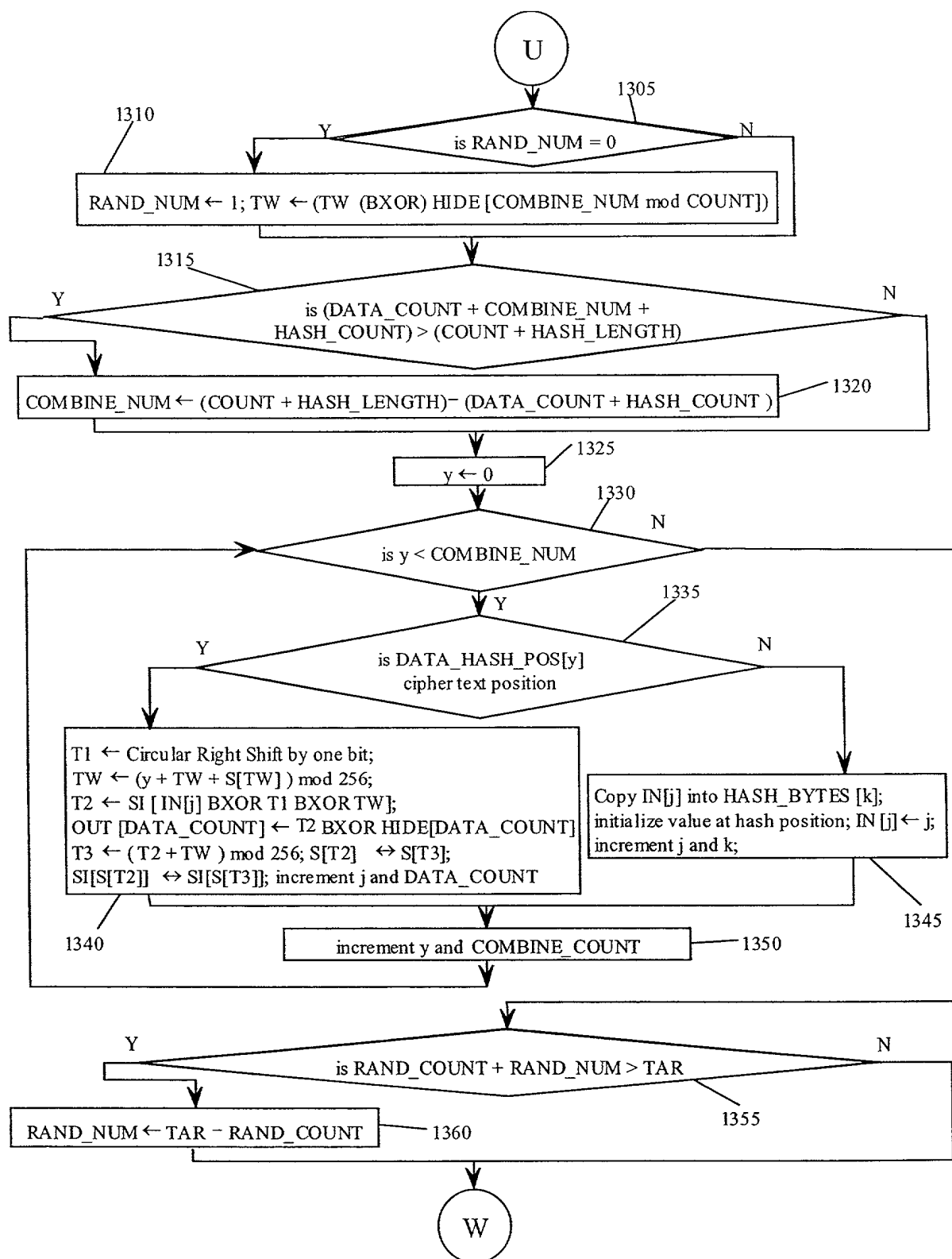


Figure 21

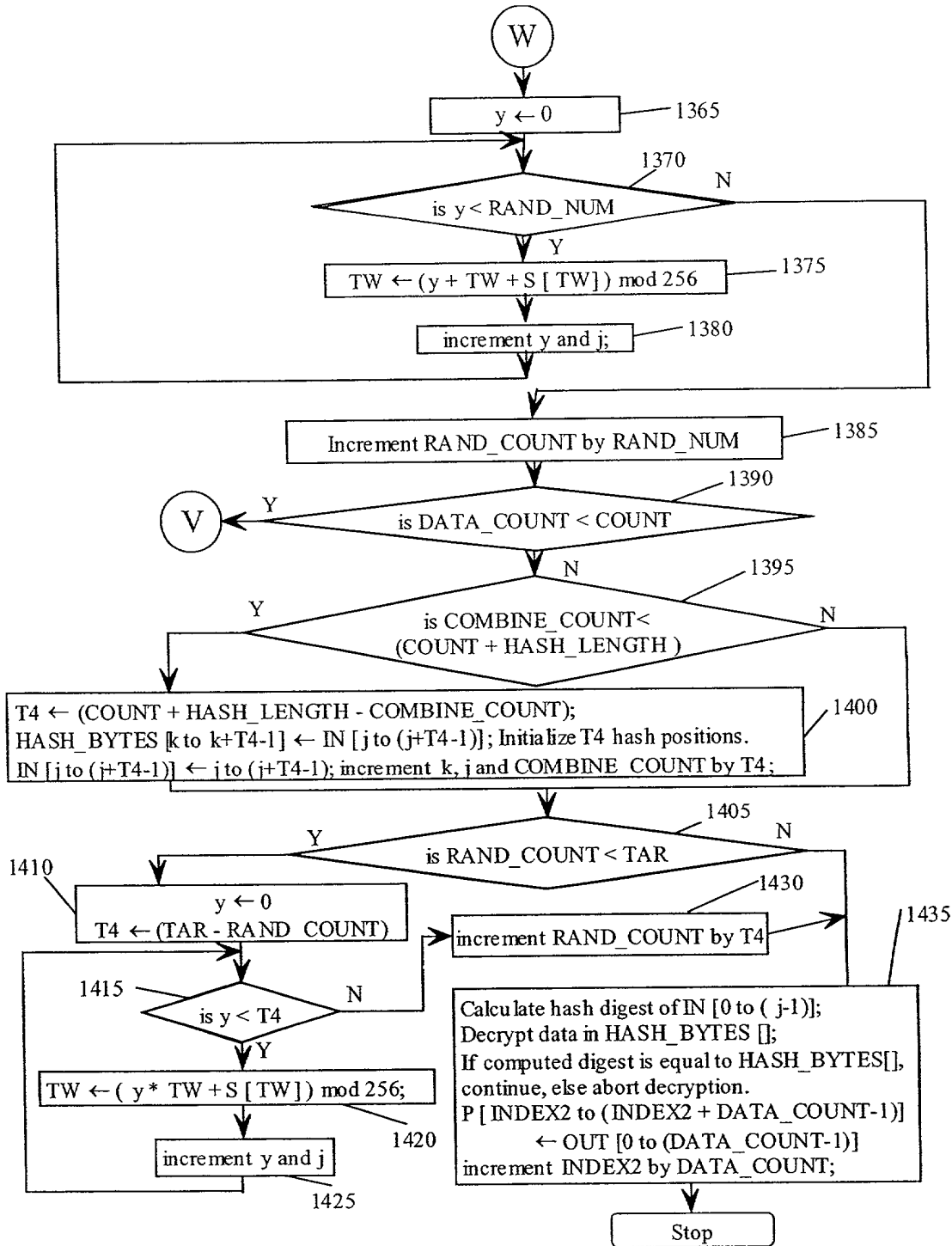


Figure 22

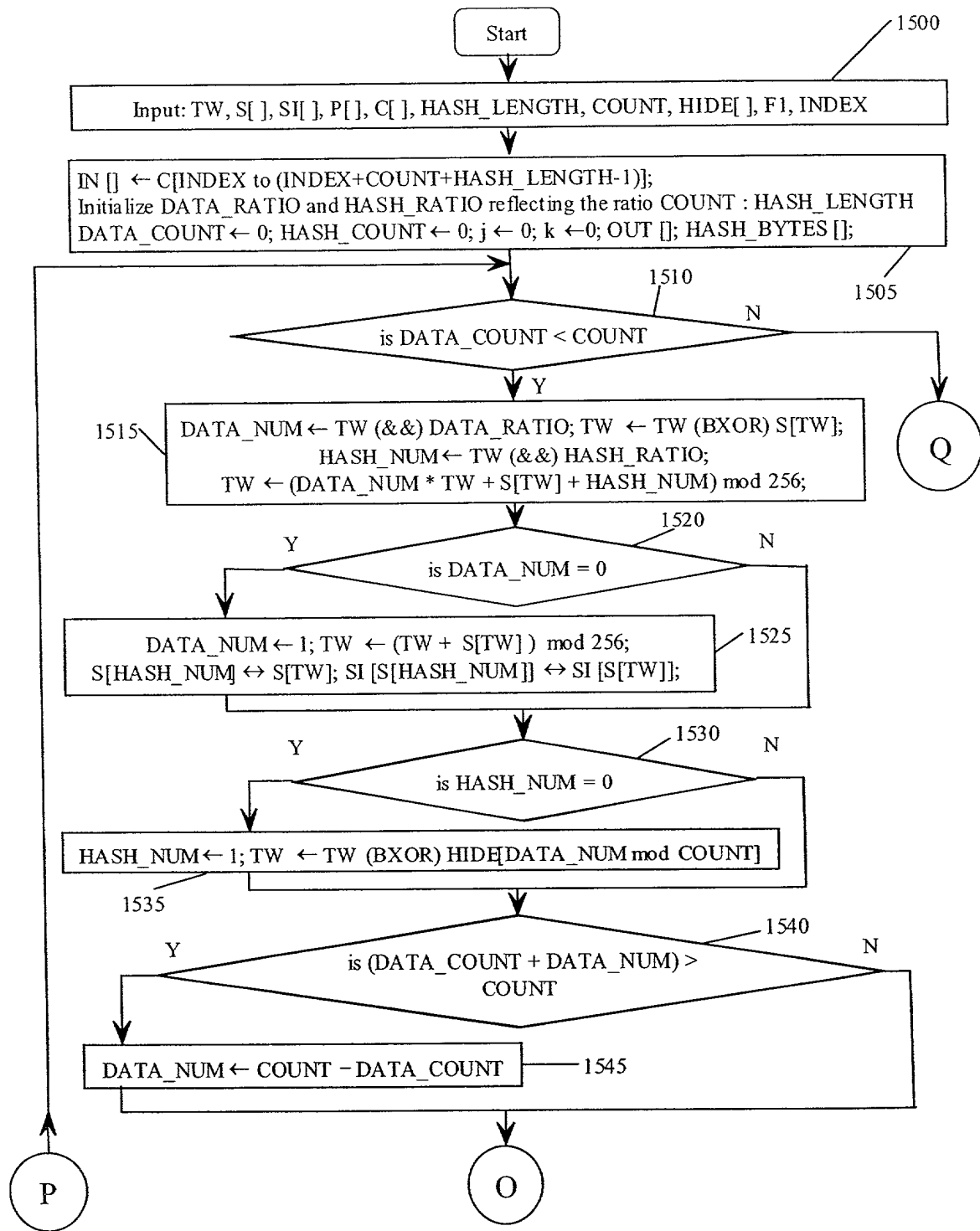


Figure 23

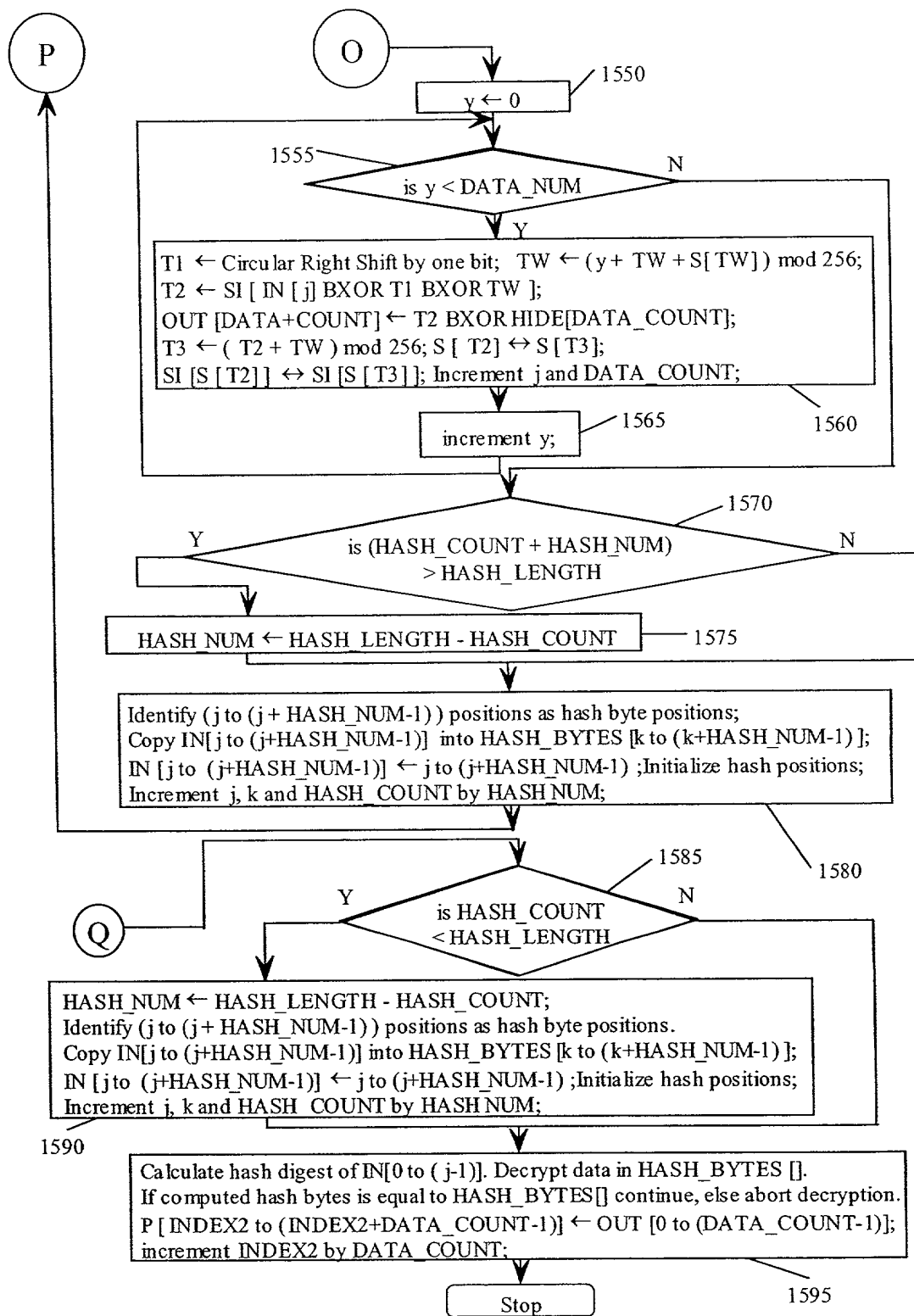


Figure 24

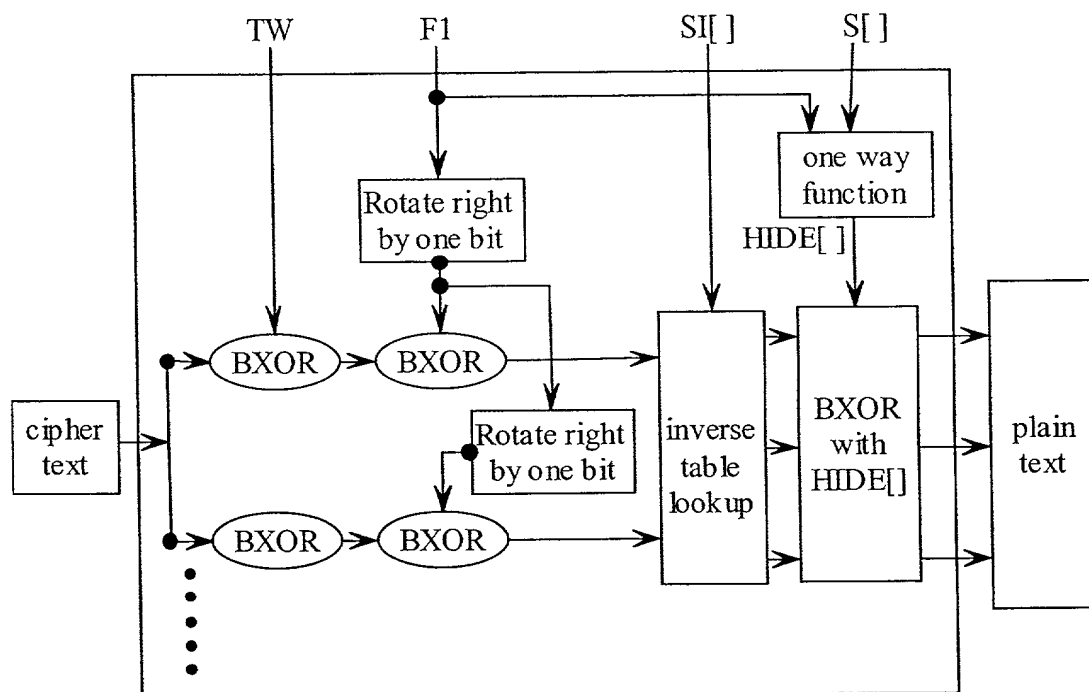


Figure 25

FIG. 26 is a block diagram of a system 1600 illustrating a source computing device (smart card) 1610<sub>1</sub> and a target computing device 1620. The source computing device 1610<sub>1</sub> includes an IC 1630<sub>1</sub> and memory 1640<sub>1</sub>, which includes an IID 1650<sub>1</sub>. The target computing device 1620 is connected to the source computing device 1610<sub>1</sub> and the source computing device 1610<sub>M</sub>. The system 1600 is enclosed in a dashed box.

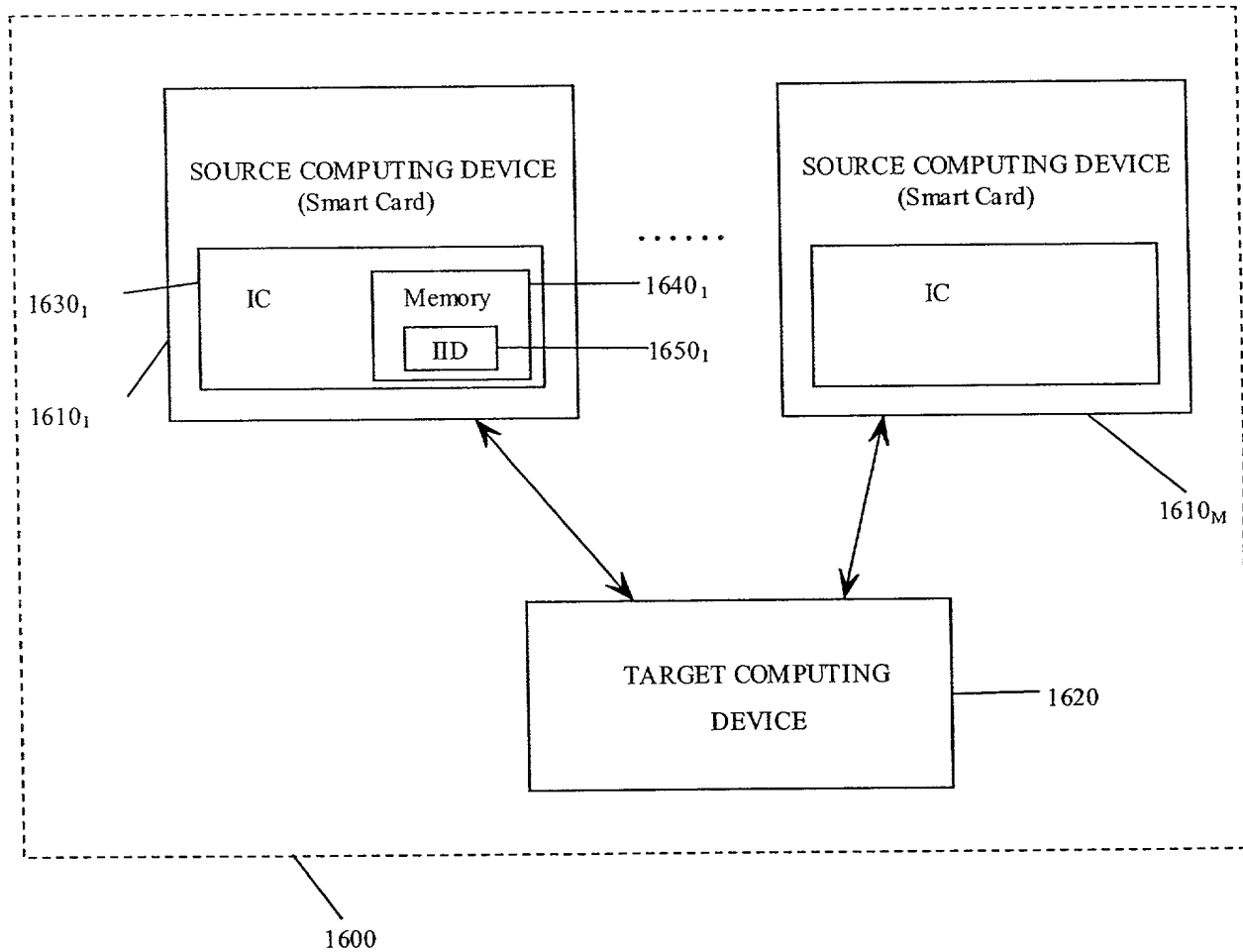
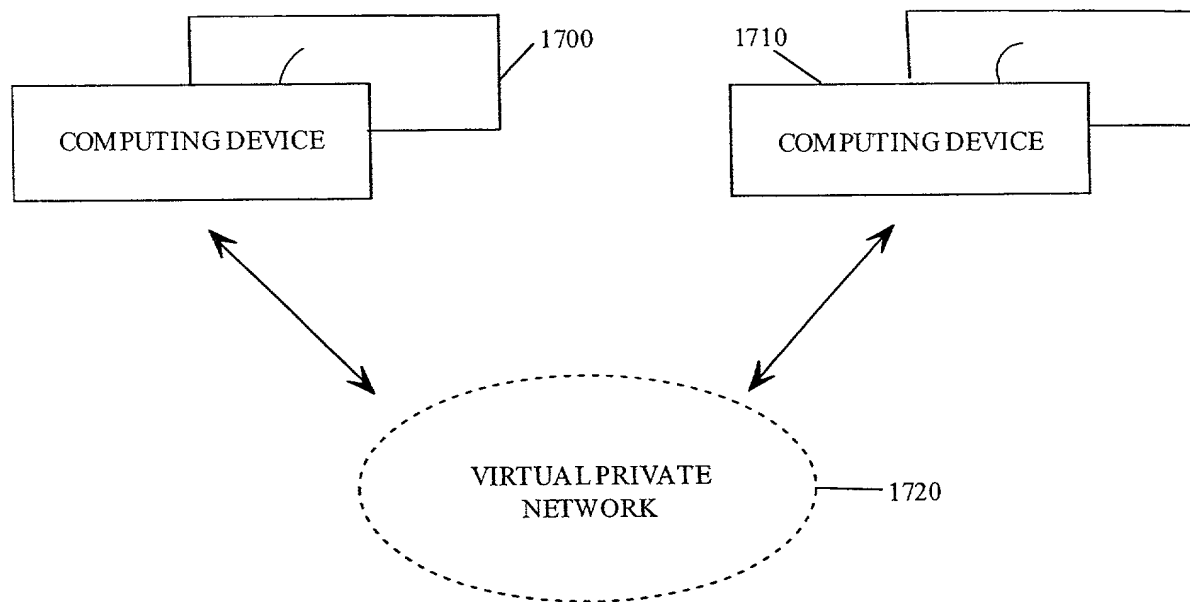


Figure 26



**Figure 27**



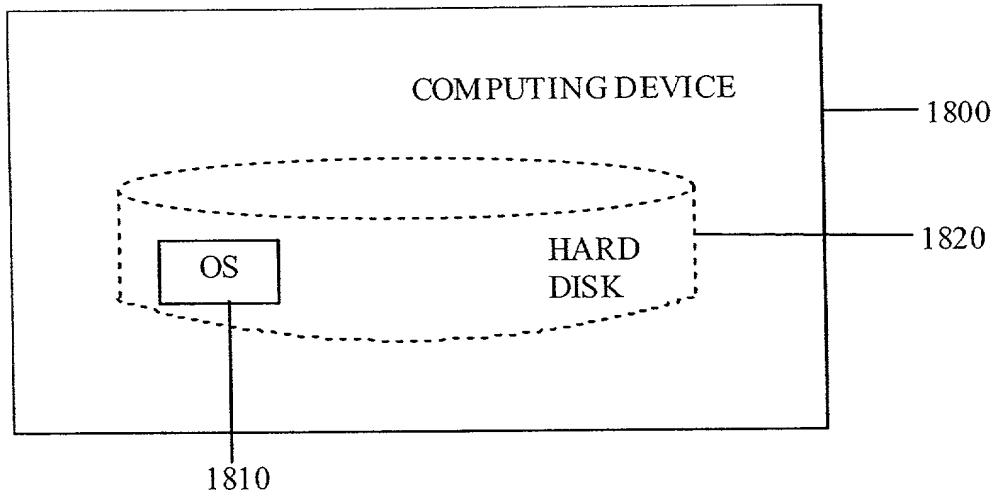


Figure 28

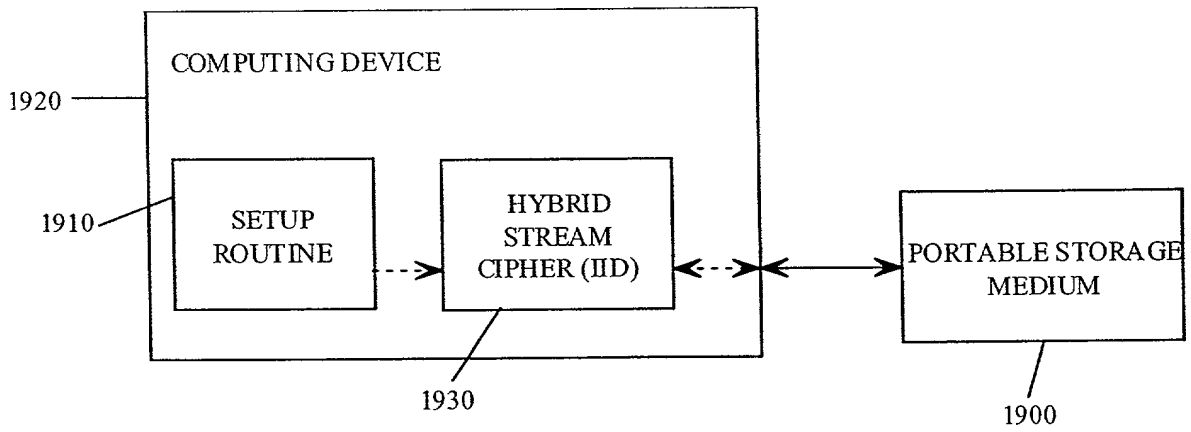


Figure 29

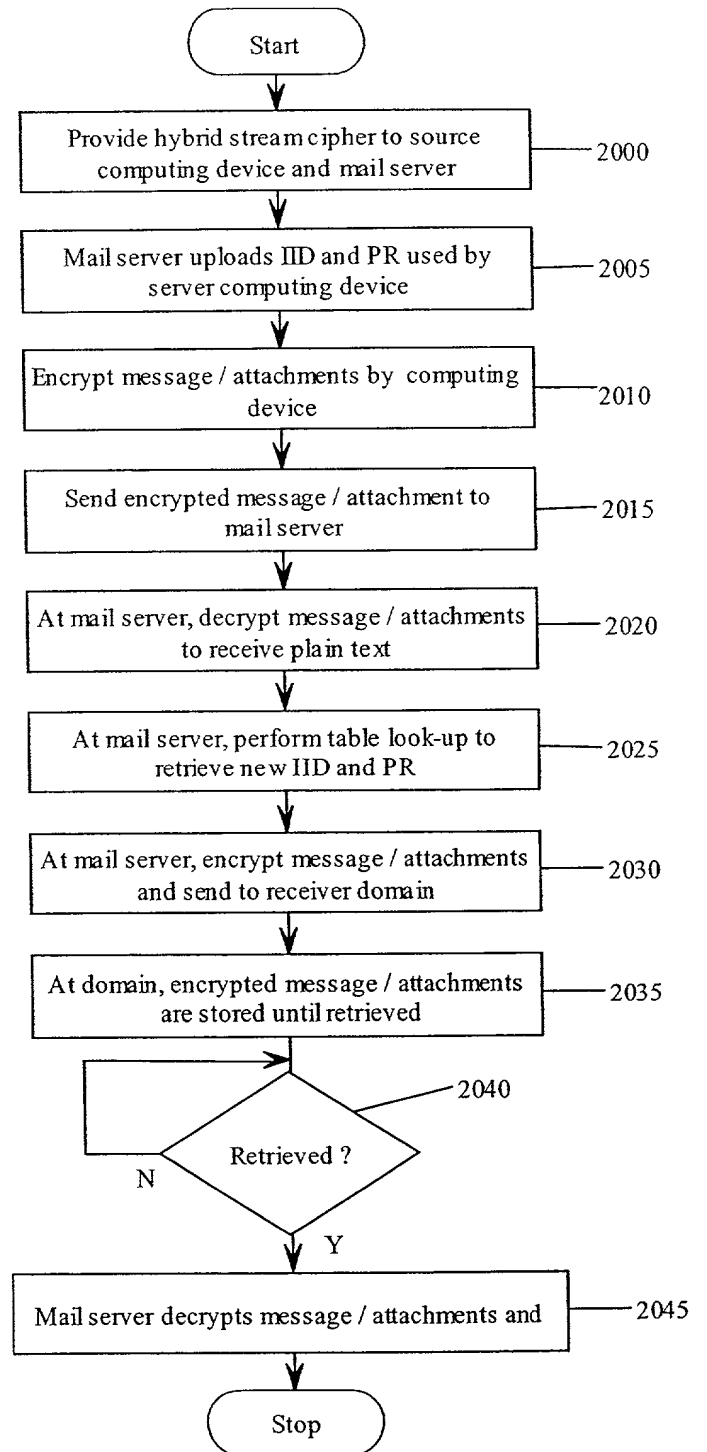
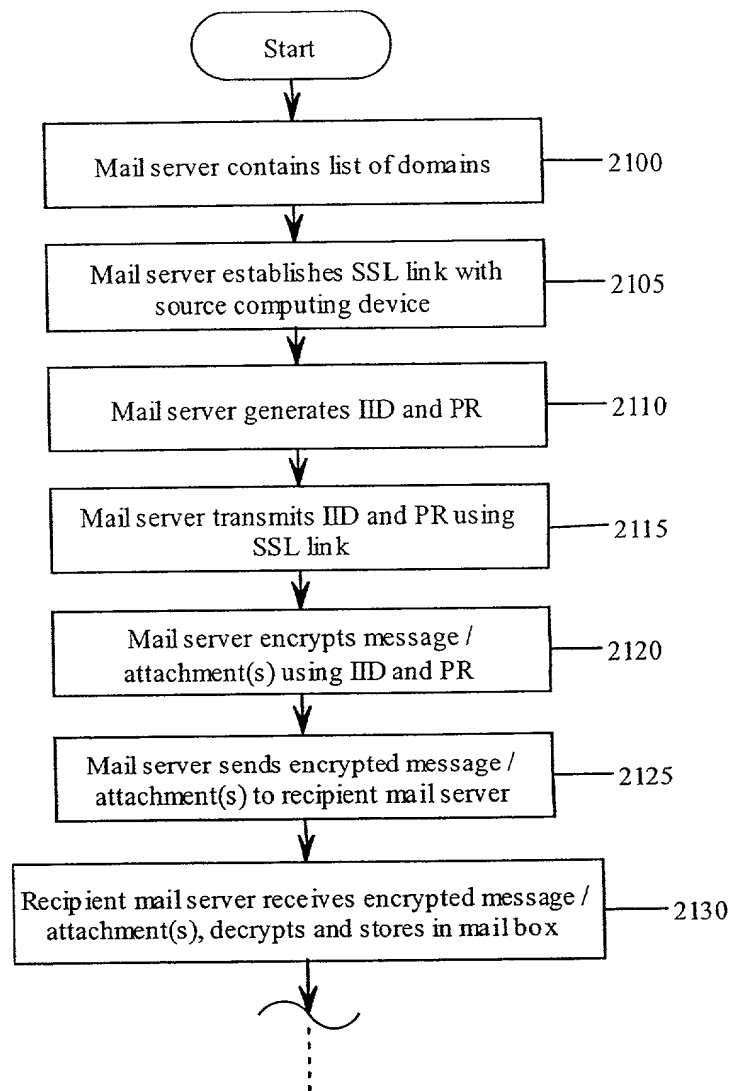


Figure 30



**Figure 31**

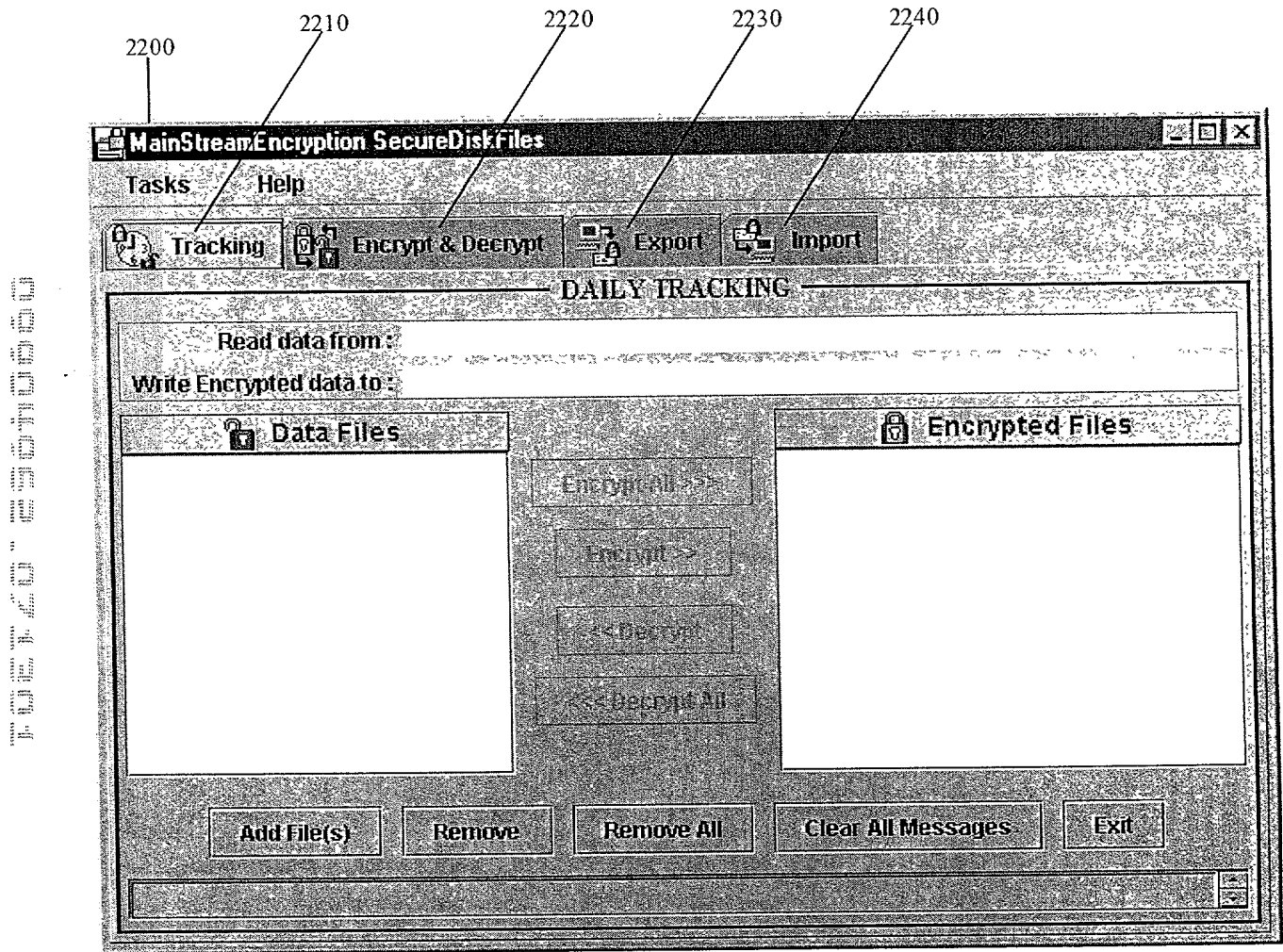


Figure 32

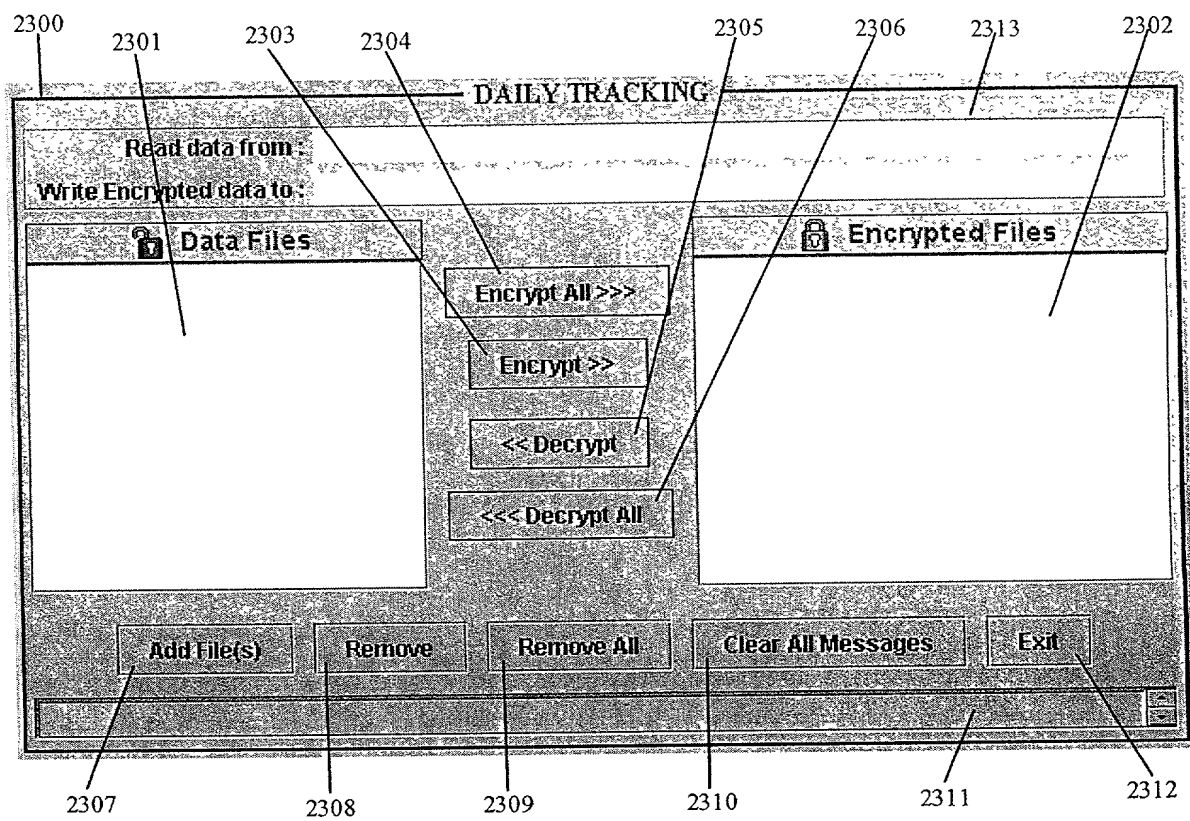


Figure 33

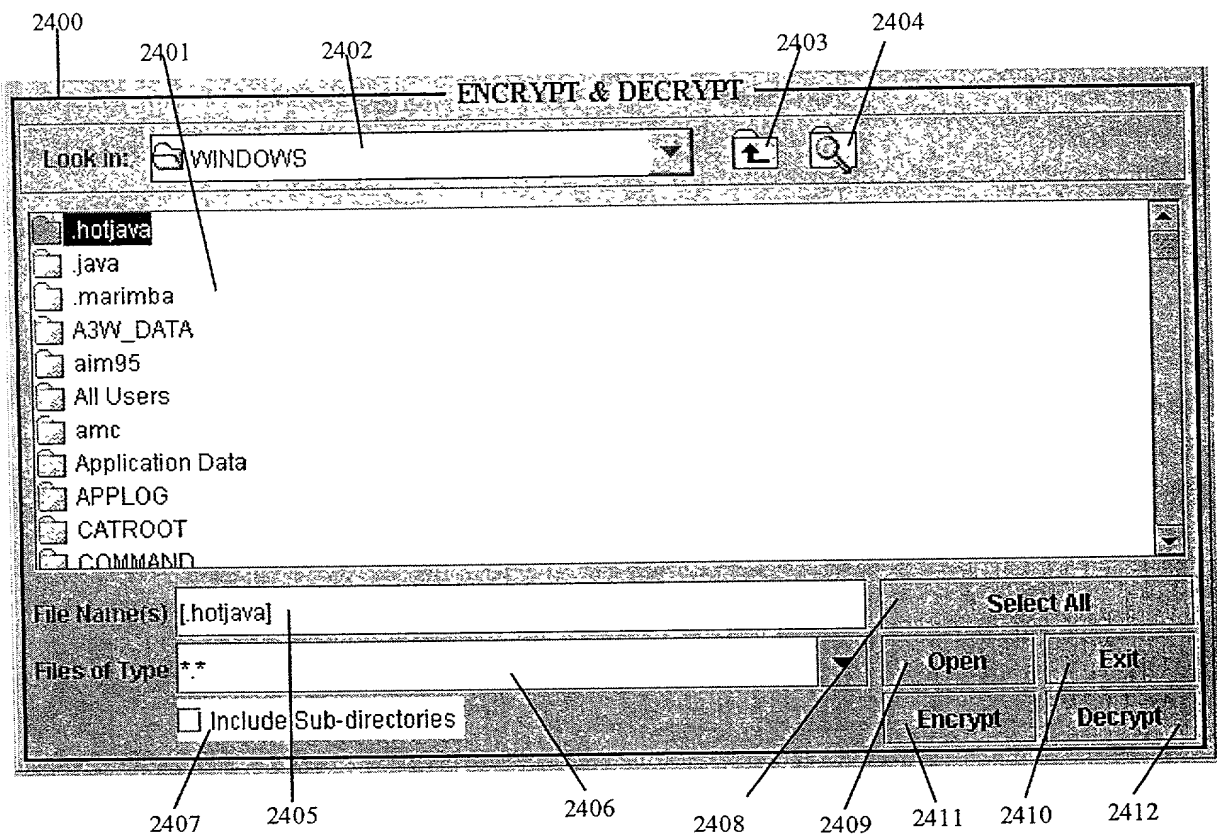


Figure 34

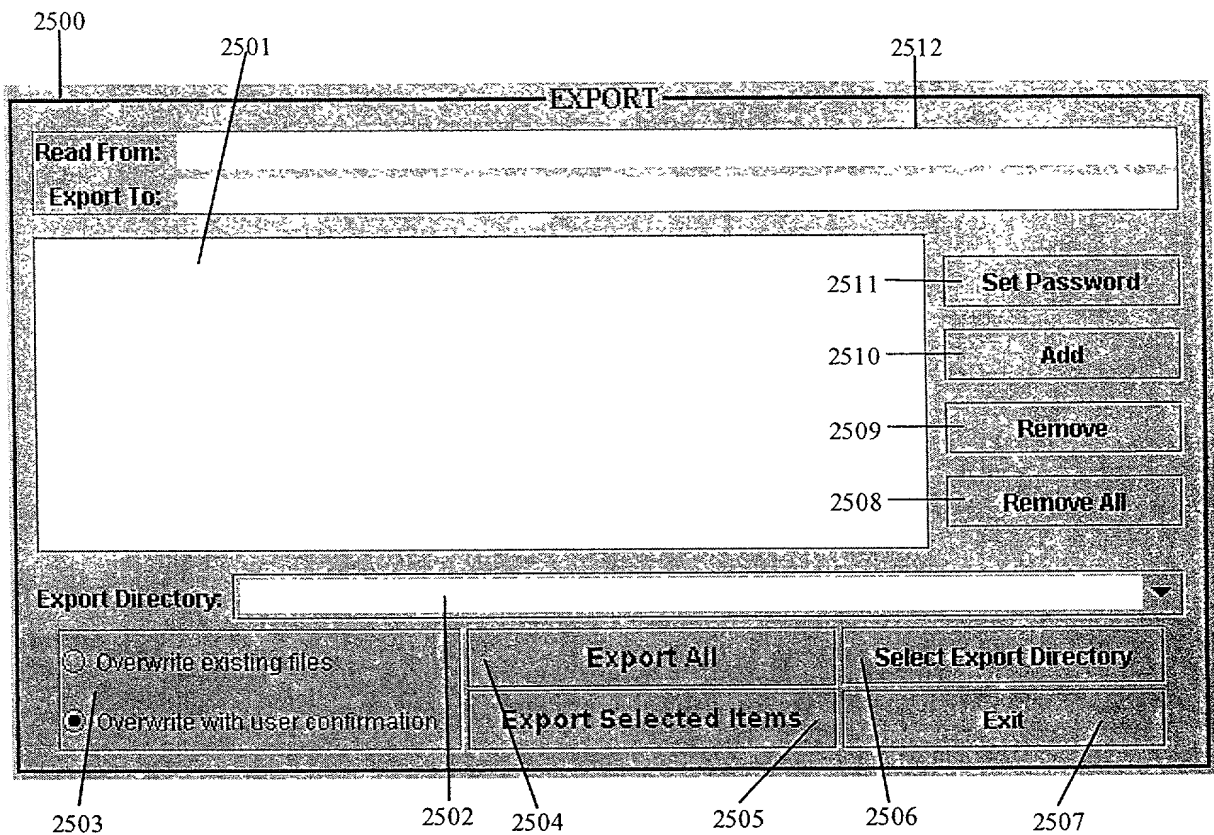


Figure 35

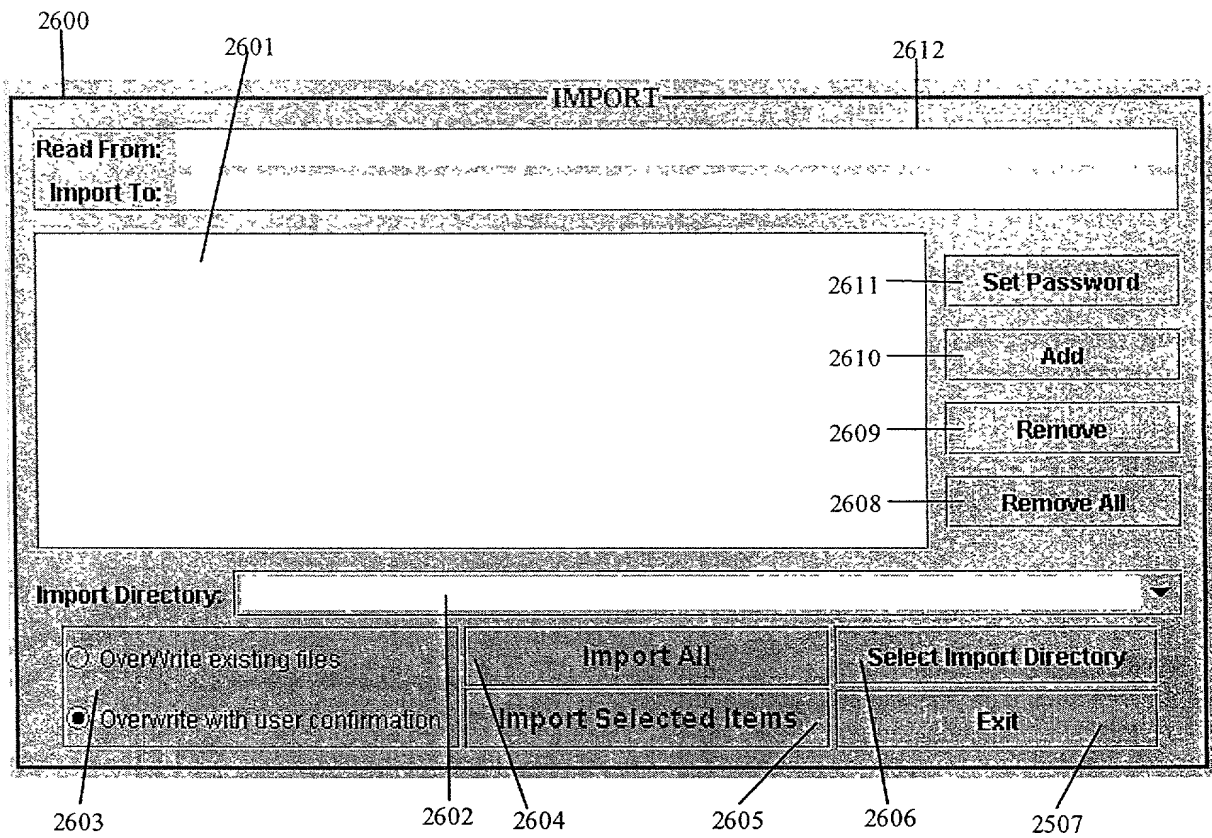


Figure 36



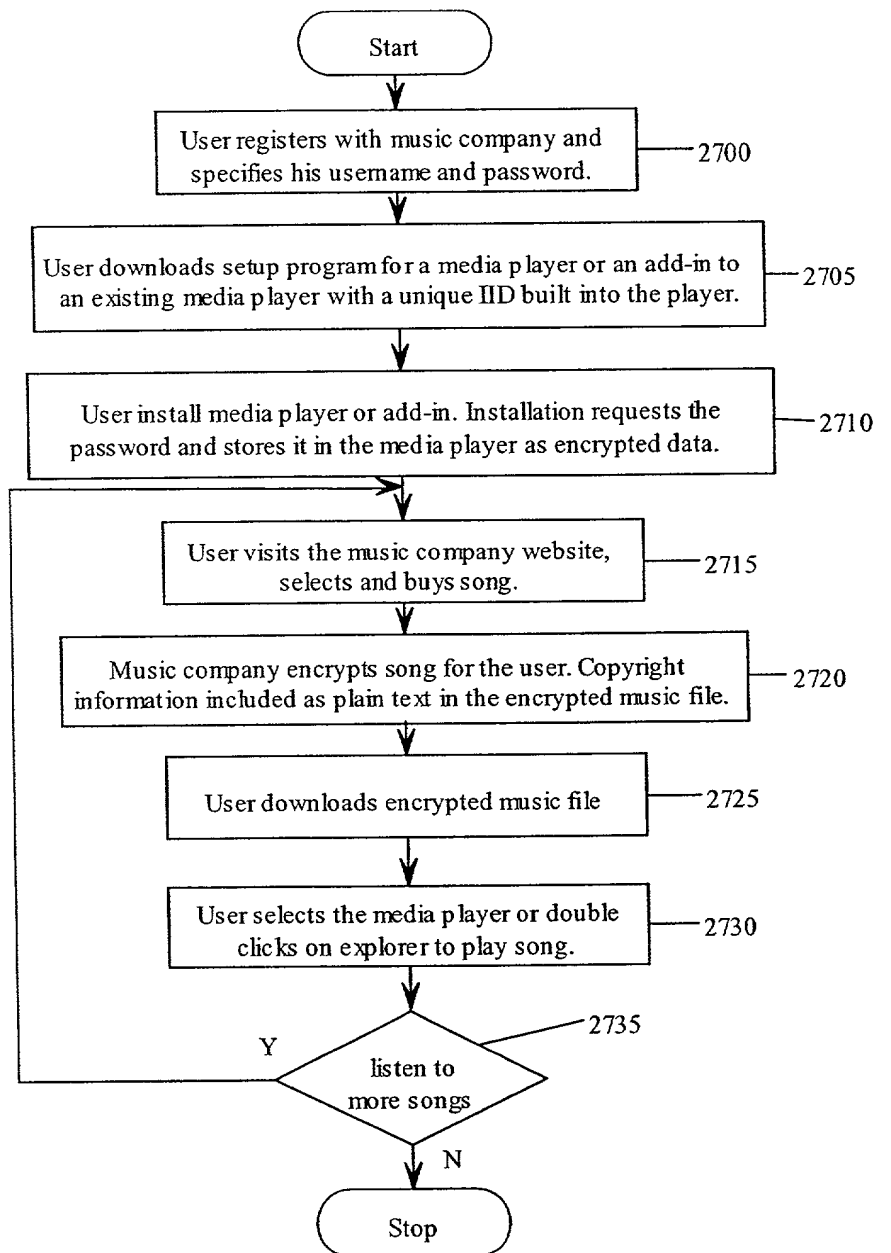


Figure 37